

01/18/2002

Serial No.:09/863,927

SYSTEM:OS - DIALOG OneSearch  
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File 305:Analytical Abstracts 1980-2002/Jan W2  
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\*File 305: Frequency of updates and Alerts changing to weekly.  
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File 315:ChemEng & Biotec Abs 1970-2002/Dec  
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(c) 2002 Cambridge Sci Abs  
File 65:Inside Conferences 1993-2002/Jan W2  
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Set	Items	Description
S1	1389283	IC OR ICS OR INTEGRATED(W)CIRCUIT? ? OR (MICRO) (W) (CIRCUIT? ? OR CHIP? ?) OR CHIP? ? OR MICROCIRCUIT? ? OR DIE? ?
S2	71079	CC=B2570 Semiconductor integrated circuits
S3	478223	DIELECTRIC?
S4	158104	CURING OR CURABLE OR CURE OR CURED
S5	3481241	(ASSEMBLED OR CONSTRUCT? OR FABRICAT? OR MANUFACTUR? OR MO-LD)
S6	4397048	(PACKAGE? OR ENCAS????? OR PROTECT? OR CASING OR CASE OR C-AVITY OR ENCAPSULAT? OR CAPSUL?)
S7	152026	(S1 OR S2) AND S6
S8	3202	S7 AND S3
S9	3	S8 AND ((CURING OR CURABLE OR CURE OR CURED) (5N) (LIQUID? ? - OR FLUID? ? OR SOL? ? OR SOLUTION? ? OR SOLN))
S10	2	RD (unique items)
S11	16	S8 AND ((CURING OR CURABLE OR CURE OR CURED) (S) (LIQUID? ? OR FLUID? ? OR SOL? ? OR SOLUTION? ? OR SOLN))
S12	15	RD (unique items)
S13	33942	S7 AND (S5 OR MOLDED OR MOLDING OR ASSEMBL?)
S14	1353	S13 AND S3
S15	11	S14 AND ((CURING OR CURABLE OR CURE OR CURED) (S) (LIQUID? ? OR FLUID? ? OR SOL? ? OR SOLUTION? ? OR SOLN))
S16	16	S10 OR S12 OR S15
S17	15	RD (unique items)
S18	21	S14 AND ((CURING OR CURABLE OR CURE OR CURED) (S) (ELASTOMER? OR RUBBER OR POLYMER? OR PLASTIC OR THERMOPLASTIC?))
S19	18	RD (unique items)
S20	2942798	(ASSEMBL? OR CONSTRUCT? OR FABRICAT?)
S21	21977	S7 AND S20
S22	944	S21 AND DIELECTRIC?
S23	13	S22 AND ((CURING OR CURABLE OR CURE OR CURED) (S) (ELASTOMER? OR RUBBER OR POLYMER? OR PLASTIC OR THERMOPLASTIC?))
S24	11	RD (unique items)
S25	10	S22 AND ((CURING OR CURABLE OR CURE OR CURED) (S) (LIQUID? ? OR FLUID? ? OR SOL? ? OR SOLUTION? ? OR SOLN))
S26	9	RD (unique items)
S27	127	S7 AND SUBASSEMBL?
S28	3	S27 AND DIELECTRIC?
S29	3	RD (unique items)
S30	25092	(S1 OR S2) AND DIELECTRIC?
S31	3202	S30 AND S6
S32	0	S31 AND ((COMPLIANT) (3N) (LAYER? OR FILM? ? OR COAT????))
S33	25	(S19 OR S24 OR S26)
S34	25	RD (unique items)
S35	5	S17 NOT S34
?		

34/3,AB/3 (Item 3 from file: 2)  
DIALOG(R)File 2:INSPEC

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6595799 INSPEC Abstract Number: B2000-06-0170J-095  
Title: Characteristics and reliability of no-flow underfills for solder  
bumped flip chip assemblies

Author(s): Lau, J.H.; Chang, C.; Chih-Chiang Chen  
Author Affiliation: Express Packaging Syst. Inc., Palo Alto, CA, USA

Journal: International Journal of Microcircuits and Electronic Packaging  
vol.22, no.4 p.370-81  
Publisher: IMAPS-Int. Microelectron. & Packaging Soc,

Publication Date: 1999 Country of Publication: USA  
CODEN: IMEPES ISSN: 1063-1674

SICI: 1063-1674(1999)22:4L:370:CRFU;1-5  
Material Identity Number: P802-2000-002

Language: English

Abstract: Solder bumped flip chips on low cost substrates with three different epoxy-based no-clean flux liquid-like no-flow underfills are presented in this study. This paper includes evaluation of three commercial no-flow underfills and characterization of material and process parameters. Important materials and process parameters, such as curing temperature and time, coefficient of thermal expansion, storage modulus, loss modulus, tan delta, glass transition temperature, moisture uptake, solder reflow, and post curing are discussed in this work. The curing mechanism during reflow of no-flow underfills is illustrated in this paper and a comparison of no-flow underfill and conventional underfill is also addressed. Also, cross-sections are examined for a better understanding of the effects of these no-flow underfill materials on the interconnects of the flip chip assemblies. Shear and thermal cycling tests and results for these flip chip assemblies are reported and analyzed.

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34/3,AB/4 (Item 4 from file: 2)  
DIALOG(R)File 2:INSPEC  
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6572700 INSPEC Abstract Number: B2000-06-2550F-007

Title: Low-k porous spin-on-glass  
Author(s): Kohl, P.A.; Padovani, A.; Wedlake, M.; Bhusari, D.; Bidstrup  
Allen, S.A.; Shick, R.; Rhodes, L.  
Author Affiliation: Sch. of Chem. Eng., Georgia Inst. of Technol.,  
Atlanta, GA, USA  
Conference Title: Low-Dielectric Constant Materials V. Proceedings  
(Materials Research Society Symposium Proceedings Vol.565) p.55-61  
Editor(s): Hummel, J.; Endo, K.; Lee, W.W.; Mills, M.; Wang, S.-Q.  
Publisher: Mater. Res. Soc, Warrendale, PA, USA  
Publication Date: 1999 Country of Publication: USA xi+306 pp.  
ISBN: 1 55899 472 6 Material Identity Number: XX-2000-00483  
Conference Title: Low-Dielectric Constant Materials V. Symposium  
Conference Date: 5-8 April 1999 Conference Location: San Francisco,  
CA, USA

Language: English

Abstract: Previously, the fabrication of air-gap structures for electrical interconnections was demonstrated using a sacrificial polymer encapsulated in conventional dielectric materials. The air-gaps were formed by thermally decomposing the sacrificial polymer and allowing the by-products to diffuse through the encapsulating dielectric. The diffusivity of the polymer decomposition products is adequate at elevated temperatures to allow the formation of air-gaps. This process was extended to form low dielectric constant porous silica from commercially available methylsilsesquioxane (MSQ) by the addition of the sacrificial polymer to the MSQ. The porous MSQ film was thermally cured followed by decomposition of the norbornene (NB) polymer at temperatures above 400 degrees C. The dielectric constant of the MSQ was lowered from 2.7 to 2.3 by creating 70 nm pores in the MSQ. The voids created in the MSQ appeared to exhibit a closed-pore structure.

34/3,AB/5 (Item 5 from file: 2)  
DIALOG(R)File 2:INSPEC  
(c) 2002 Institution of Electrical Engineers. All rts. reserv.

6491892 INSPEC Abstract Number: B2000-03-2250-009

Title: Reducing polyimide cure time for MCM-D  
Author(s): Wilkins, W.; Schuckert, C.  
Author Affiliation: New Technol. Lab., Union Semicond. Technol. Corp.,  
Chippewa Falls, WI, USA  
Journal: Advanced Packaging vol.8, no.10 p.42-6  
Publisher: IHS Publishing Group,  
Publication Date: Nov.-Dec. 1999 Country of Publication: USA  
CODEN: ADPAFZ ISSN: 1065-0555  
SICI: 1065-0555(199911/12)8:10L:42:RPCT;1-M  
Material Identity Number: F109-2000-001  
U.S. Copyright Clearance Center Code: 1065-0555/99/\$1.00+.50  
Language: English  
Abstract: Polyimides are commonly used as both inner layer dielectrics and as the solder dam in the fabrication of multichip module deposited dielectric (MCM-D) packages. The New Technology Laboratory (NTL) used PI-2611 polyimide as a thin film dielectric to make MCMs. This polymer was chosen for its

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low-stress properties, high modulus and close coefficient of thermal expansion match to silicon. However, the cure cycle that was initially implemented into production was very long. As production volumes increased, it became desirable to shorten the curing process. This article reviews the following: MCM product applications; PI-2611 polyimide and its applicability in the fabrication of thin film multilayer packages; the experimental design to test the shortened polyimide cure cycles; and the resulting effects on stress, adhesion and dielectric constant.

34/3,AB/6 (Item 6 from file: 2)

DIALOG(R)File 2:INSPEC

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6364416 INSPEC Abstract Number: B1999-11-0170J-041

Title: Development and application by ink-jet printing of advanced packaging materials

Author(s): Hayes, D.J.; Grove, M.E.; Cox, W.R.

Author Affiliation: MicroFab Technol. Inc., Plano, TX, USA

Conference Title: Proceedings International Symposium on Advanced Packaging Materials. Processes, Properties and Interfaces (IEEE Cat. No.99TH8405) p.88-93

Publisher: IMAPS - Int. Microelectron. & Packaging Soc, Reston, VA, USA

Publication Date: 1999 Country of Publication: USA vii+362 pp.

ISBN: 0 930815 56 4 Material Identity Number: XX-1999-00906

Conference Title: Proceedings International Symposium on Advanced Packaging Materials. Processes, Properties and Interfaces

Conference Sponsor: Int. Microelectron. & Packaging Soc. (IMAPS); IEEE Components, Packaging, & Manuf. Technol. (CPMT); Georgia Inst. Technol., Packaging Res. Center (PRC)

Conference Date: 14-17 March 1999 Conference Location: Braselton, GA, USA

Language: English

Abstract: High temperature ink-jet based printing processes (MicroJet) and custom polymer formulations have been developed for use in the fabrication of high-density microelectronic and optoelectronic packages. The enabling technologies for this work have been the development of a high-temperature (to 300 degrees C) print head and a set of UV-curing polymeric and oxide-filled formulations satisfying the rheological requirements for application by MicroJet. MicroJet processes have been utilized in the printing of solder bumps and vias, micro-optical interconnects, dielectric coatings, passive microelectronic elements, and adhesives. Potential applications of MicroJet processes and materials include: integrated circuit and chip-scale packaging, optical interconnect fabrication, printed wiring board manufacturing, and flat panel display assembly. The inherently data-driven nature of MicroJet processes lead to higher levels of process integration, lower costs, and increased manufacturing flexibility. Commercial platforms exist for print-on-the-fly solder deposition at rates of over 400 bumps/sec, and similar systems for high speed printing of polymers are under development. The range of packaging applications addressable by MicroJet technology is set to expand rapidly as printable feature sizes are reduced and as new MicroJetable material formulations are developed to meet a growing set of applications.

34/3,AB/7 (Item 7 from file: 2)

DIALOG(R)File 2:INSPEC

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6335415 INSPEC Abstract Number: B1999-10-2250-004

Title: Sequential modeling of via formation in photosensitive dielectric materials for MCM-D applications

Author(s): Tae Seon Kim; May, G.S.

Author Affiliation: Sch. of Electr. & Comput. Eng., Georgia Inst. of Technol., Atlanta, GA, USA

Journal: IEEE Transactions on Semiconductor Manufacturing vol.12, no.3 p.345-52

Publisher: IEEE,

Publication Date: Aug. 1999 Country of Publication: USA

CODEN: ITSMED ISSN: 0894-6507

SICI: 0894-6507(199908)12:3L:345:SMFP;1-L

Material Identity Number: M512-1999-003

U.S. Copyright Clearance Center Code: 0894-6507/99/\$10.00

Language: English

Abstract: Multichip module (MCM) technology is considered a strategic solution in electronics packaging because this approach offers significant advantages in electrical and thermal performance and reliability. However, manufacturing cost is a critical issue for mass production of high-performance MCM packages. To realize low-cost manufacturing technology, process modeling, optimization, and control techniques are required. In this paper, a modeling approach for via formation in MCM dielectric layers composed of photosensitive benzocyclobutene (BCB) is presented. A series of designed experiments are used to characterize the via formation workcell (which consists of the spin coat, soft bake, expose, develop, cure, and plasma descum unit process steps). The output characteristics considered are film thickness, refractive index, uniformity, film retention, and via yield. Sequential neural network process models are constructed to characterize the entire process. In the sequential scheme, each workcell subprocess is modeled individually, and each subprocess model is linked to previous subprocess outputs and subsequent subprocess inputs. This modeling scheme is compared with both the global and unit process modeling approaches to evaluate model prediction capability. The sequential method shows superior capability, with an average rms prediction error of 6.40% over all responses, compared to a 11.61% rmse for the global model and a 12.05% error for the unit process models.

Subfile: B

34/3,AB/10 (Item 10 from file: 2)  
DIALOG(R)File 2:INSPEC  
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5893589 INSPEC Abstract Number: B9805-0170J-055

Title: Elastomeric conformal coatings improve reliability of integrated circuits

Author(s): Krueger, M.G.

Author Affiliation: Dow Corning Corp., Midland, MI, USA

Conference Title: Proceedings of the Technical Program. NEPCON West '96

Conference Part vol.1 p.479-84 vol.1

Publisher: Reed Exhibition, Norwalk, CT, USA

Publication Date: 1996 Country of Publication: USA 3 vol. 1810 pp.

Material Identity Number: XX95-03168

Conference Title: Proceedings of Nepcon West 96

Conference Date: 27-29 Feb. 1996 Conference Location: Anaheim, CA, USA

Language: English

Abstract: Several forces are driving the development of new conformal coating materials, including environmental, performance and processing issues. Of primary importance is the increasing regulation of volatile organic compounds (VOCs) at federal, state and local levels. Current and anticipated legislation is dictating the elimination of solvent carriers, and encouraging the use of no-clean process technology. At the same time, increased miniaturization of new circuit board designs requires flexible, low-stress coating materials to **protect** delicate components and fine-pitch leads. Excellent humidity resistance and good **dielectric** properties over a wide temperature range remain high priorities. From a processing standpoint, one-part, primerless formulations are increasingly in demand as OEMs seek to simplify operations and boost output. The ability to heat-accelerate **cure** is important for reduced cycle time in some applications, while room-temperature **cure** and quick tack-free handling are necessary in others. In nearly all situations, OEMs and contract coaters require the new materials to be compatible with existing process equipment. Conformal coatings and encapsulants based on silicone technology have been used for many years. Like most products for these applications, the materials have been primarily solvent-based. However, a new line of solventless silicone coatings has been developed by Dow Corning Corporation, which **cure** to a low-stress **elastomer** designed to **protect** rigid and flexible printed wiring boards (PWBs). Room-temperature vulcanizing (RTV) moisture **cure** materials and thermal **cure** products are available.

34/3,AB/11 (Item 11 from file: 2)  
DIALOG(R)File 2:INSPEC  
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5665003 INSPEC Abstract Number: B9709-2250-006

Title: Embedding technology-a **chip**-first approach using BCB

Author(s): Topper, M.; Buschick, K.; Wolf, J.; Glaw, V.; Hahn, R.; Dabek, A.; Ehrmann, O.; Reichl, H.

Author Affiliation: Tech. Univ. Berlin, Germany

Conference Title: Proceedings. 3rd International Symposium on Advanced Packaging Materials Processes, Properties and Interfaces (Cat. No.97TH8263) p.11-14

Publisher: IEEE, New York, NY, USA

Publication Date: 1997 Country of Publication: USA viii+183 pp.

ISBN: 0 7803 3818 9 Material Identity Number: XX97-00693

Conference Title: Proceedings 3rd International Symposium on Advanced

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Packaging Materials Processes, Properties and Interfaces

Conference Sponsor: Int. Microelectron. & Packaging Soc. (IMAPS); IEEE Components, Packaging, & Manuf. Technol. Soc.; Georgia Inst. Technol., Packaging Res. Center (PRC)

Conference Date: 9-12 March 1997 Conference Location: Braselton, GA, USA

Language: English

Abstract: With the current trend to ever faster clock rates the propagation delays between the **chips** constitute a significant portion of the clock cycle. Mounting both active and passive devices as closely together as possible will therefore boost system's performance. Although flip-chipped devices have good performance, design constraints may prevent the placement of pads to comply with flip chip design rules. An additional advantage of the embedding technology is the possibility to employ 3-D stacking, the highest **package** density. Bare dice and standard passive components were embedded into a ceramic substrate to achieve a common, planar surface. Hence by employing thin-film processing all components can be directly interconnected to the copper routing of the module. Benzocyclobutene (BCB) with its low **curing** temperature is preferred as **dielectrical polymer** for the embedding technology. Application of bonding or soldering techniques which might limit the reliability is avoided. This offers excellent electrical properties of the wiring system. By planarizing the reverse side of the MCM a low thermal resistance between heat sink and dice can be accomplished simultaneously for all embedded components. An SRAM MCM and a Thermotest MCM demonstrate the feasibility of the embedding technology.

34/3,AB/13 (Item 13 from file: 2)

DIALOG(R)File 2:INSPEC

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4823423 INSPEC Abstract Number: B9412-0170J-067

Title: Development of a cost effective high performance metal QFP packaging system

Author(s): Mahulikar, D.; Pasqualoni, A.; Crane, J.; Braden, J.

Author Affiliation: Metals Res. Labs., Olin Corp., New Haven, CT, USA p.405-11

Publisher: IEEE, New York, NY, USA

Publication Date: 1993 Country of Publication: USA xvii+1166 pp.  
ISBN: 0 7803 0794 1

U.S. Copyright Clearance Center Code: 0569-5503/93/0000-0405\$3.00

Conference Title: Proceedings of IEEE 43rd Electronic Components and Technology Conference (ECTC '93)

Conference Date: 1-4 June 1993 Conference Location: Orlando, FL, USA

Language: English

Abstract: This paper describes the design and development of MQUAD technology. The MQUAD packaging system is a high performance reliable technology currently in use for packaging of microprocessors, high-speed ASIC devices, including CMOS, Bi CMOS, Bi polar, gallium arsenide, and other high performance IC's. The packaging technology is being used for devices dissipating up to 14 watts and switching speed of up to 300 MHz. The design and development was carried out with the objectives of high thermal performance (up to 15 watts), high electrical performance (inductance and capacitances lower than comparable PQFPs) and reliability superior to the PQFPs. The approach taken was; to use an adhesively bonded metal **package**. An aluminum alloy lid and base were chosen to give excellent heat dissipation ability, mechanical integrity and light weight **construction**. A special anodization process was developed to put a hard, electrically insulating black colored anodic film on the aluminum



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alloy components. The adhesive seal is a filled epoxy having low dielectric constant and low ionic content and with excellent adhesion to both copper alloys and aluminum anodic films, especially in moist environments. The leadframe chosen is a high-strength, thermally conductive copper alloy. The assembly process for the MQAD package emulates the PQFP assembly process except that the molding step is replaced by a single step pad attach simultaneous with the seal adhesive lamination/cure process. The leadframe pad is attached to the anodized aluminum alloy base via a silver-filled epoxy paste. The package was thoroughly tested for reliability and fully characterized for thermal and electrical performance. Reliability tests performed include temperature cycling, thermal shocks, solvent resistance, flammability, pressure cooker, and vapor phase shocks. Reliability of MQAD packages is superior to that of PQFPs. Characterization includes theta /sub ja/ and theta /sub jc/, and resistance, inductance and capacitance measurements. Thermal and electrical performance of MQAD packages equal or exceed that of comparable plastic or ceramic QFPs. The high reliability and performance of MQAD was confirmed by many customers and users and has been published. Because of these benefits, the technology is being further extended to advanced packages such as MCMs, TAB and ball or pad grid arrays.

34/3,AB/14

(Item 14 from file: 2)

DIALOG(R) File 2:INSPEC

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4417942 INSPEC Abstract Number: B9307-0170J-015

Title: Benzocyclobutene (BCB) dielectric for advanced MCM packaging

Author(s): Manial, T.A.; Heistand, R.H., II; Garrou, P.E.

Author Affiliation: Resin Products Tech. Services & Dev., Dow Chemical Co., Midland, MI, USA

Conference Title: Surface Mount International Conference and Exposition. Proceedings of the Technical Program p.39-47 vol.1

Publisher: Surface Mount Int, Edina, MN, USA

Publication Date: 1992 Country of Publication: USA 2 vol. 1251 pp.

Conference Date: 30 Aug.-3 Sept. 1992 Conference Location: San Jose, CA, USA

Language: English

Abstract: As designers are pushed to higher density requirements on printed wiring boards (PWB's), MCM's (multichip modules) will provide a cost effective alternative to the single chip packages. Benzocyclobutene (BCB) organic dielectrics (Cyclotene) have been introduced as high performance thermoset polymers for use in the fabrication of MCM's. Key properties for BCB in these surface mountable MCM packages are low dielectric constant (2.7), low water absorption (0.23% after 24 hr, water boil), thermal stability (350 degrees C, 1% wt. loss/hr, N2), excellent planarization (>90%), good adhesion, and a broad working temperature range (Tg>350 degrees C). Advances have been made in understanding the adhesion of BCB to substrates and interconnect metals. Adhesion promotor packages have been developed to enhance the adhesion of BCB resin onto various substrate materials such as silicon, alumina, aluminum nitride, and cofired ceramic as well as to interconnect metals such as aluminum, copper, and gold. Polymer to polymer adhesion has been enhanced by the manipulation of the cure. BCB's unique chemistry allows a thermal cure which polymerizes the resin at low temperatures in the range of 200-250 degrees C without producing any gases. This thermal cure follows an Arrhenius equation which allows for prediction of degree of cure for various time and temperature combinations.

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34/3,AB/15 (Item 15 from file: 2)  
 DIALOG(R)File 2:INSPEC  
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03523935 INSPEC Abstract Number: B90001596

Title: Finite element analysis of TAB packages

Author(s): Holalkere, V.R.

Author Affiliation: Nat. Semicond. Corp., Santa Clara, CA, USA

Conference Title: Proceedings of the Technical Program. NEPCON East '89

p.762-771

Publisher: Cahners Exposition Group, Des Plaines, IL, USA

Publication Date: 1989 Country of Publication: USA 1028 pp.

Conference Date: 13-15 June 1989 Conference Location: Boston, MA, USA

Language: English

Abstract: Mechanical and electrical problems have been observed in plastic packaged LSI devices. Electrical parametric shifts, passivation and dielectric layer cracking and shifting of metallization are some of the problems which arise after plastic encapsulation and mold cure. Preliminary reliability tests indicated voltage shifts in the devices after mold cure. This was perceived to be the result of encapsulation. The obvious solutions to decrease the die surface stresses include using low stress mold compound as well as decoupling the die surface from plastic with a thin buffer layer of soft coatings. Finite element analysis of the die, die attach pad and plastic composite was performed with and without soft coating on the die surface. The results indicated that the die surface stresses decrease in the case of the die with soft coat. Preliminary experiments on TAB packages with a soft coat on the die resulted in tape shearing off of the die. This paper addresses some of the problems associated with die coating in TAB packages.

34/3,AB/16 (Item 16 from file: 2)

DIALOG(R)File 2:INSPEC

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03118909 INSPEC Abstract Number: B88024580

Title: Simulation and analysis of thermal and microwave curing of TAB encapsulants

Author(s): Pennisi, R.

Author Affiliation: Motorola Inc., Ft. Lauderdale, FL, USA

Conference Title: Third IEEE/CHMT International Electronic Manufacturing Technology Symposium 'Manufacturing Technology - The Competitive Advantage'

(Cat. No.87CH2483 6) p.40-5

Publisher: IEEE, New York, NY, USA

Publication Date: 1987 Country of Publication: USA 257 pp.

U.S. Copyright Clearance Center Code: CH2483-6/87/0000-0040\$01.00

Conference Sponsor: IEEE

Conference Date: 12-14 Oct. 1987 Conference Location: Anaheim, CA, USA

Language: English

Abstract: In order for tape automated bonding (TAB) to be successful, numerous technologies must be brought together such that package assembly can occur in a reliable fashion. One such technology which needs to be thoroughly understood is the encapsulation of the package. Encapsulation can be accomplished by dispensing a liquid polymer onto the package and curing the polymer to a state in which its physical properties are compatible with the die and interconnect technology. A commercially available

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epoxy encapsulant was crosslinked using several curing profiles. The thermal and dielectric properties were characterized during and after the curing process. The results from these studies were used to develop an efficient curing profile using in-line infrared- and microwave-assisted curing ovens.

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/3,AB/19 (Item 3 from file: 8)  
DIALOG(R)File 8:EI Compendex(R)  
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02806579

E.I. Monthly No: EIM8910-035799  
Title: Fluorinated polyimide low **dielectric** coatings.  
Author: Ruiz, Laura M.  
Corporate Source: Ethyl Corp, Baton Rouge, LA, USA  
Conference Title: 3rd International SAMPE Electronics Conference:  
Electronic Materials and Processes  
Conference Location: Los Angeles, CA, USA Conference Date: 19890620  
E.I. Conference No.: 12425  
Source: International SAMPE Symposium and Exhibition v. Publ by SAMPE,  
Covina, CA, USA. p 209-218  
Publication Year: 1989  
CODEN: ISSEEG ISSN: 0891-0138  
Language: English

Abstract: The development of faster, more advanced integrated circuitry is placing greater demands on packaging performance. One **solution** to the need for increased speed is to place multiple **chips** in a single **package**, thereby reducing interconnect length. A critical parameter in designing such packaging is the **dielectric** material chosen. Much has been written about the use of standard polyimides (ave K equals 3.5) as **dielectrics** in IC fabrication. Polyimides are also being evaluated and used as interlevel **dielectrics** in IC packaging. Fluorinated polyimides can offer up to a 20% reduction in **dielectric** constant over standard polyimides which translates to faster signal speeds throughout the **package**. In addition to improved electrical properties, fluorinated polyimides possess less than one-third the moisture absorption of standard polyimides. This paper identifies the key performance properties of fluorinated polyimides and the benefits these properties bring to high speed packaging applications. Processability and the effect of frequency, moisture and **cure** temperature on **dielectric** constant are discussed. (Edited author abstract) 4 Refs.

34/3,AB/20 (Item 4 from file: 8)  
DIALOG(R)File 8:EI Compendex(R)  
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01090607

E.I. Monthly No: EI8202012806  
E.I. Yearly No: EI82051371  
Title: POLYIMIDE COATINGS FOR MICROELECTRONIC APPLICATIONS.  
Author: Lee, Y. K.; Craig, J. D.; Pye, W. E.  
Corporate Source: DuPont, Philadelphia, Pa, USA  
Source: Symp Proc - Univ, Gov, Ind, Microelectron Symp, 1981, Starkville, Miss, USA, May 26-28 1981 Publ by IEEE (Cat n 81CH1620-4), Piscataway, NJ, USA, 1981 p 10. 30-10. 39  
Publication Year: 1981  
Language: ENGLISH  
Abstract: The use of polyimide (PI) coatings as **dielectrics** and/or for passivation for semiconductors and thin film hybrids has become increasingly important. The principal reasons are: 1) Polyamic acids, the precursors of polyimides, are solvent soluble to give viscous **liquids** that can be spun onto a wafer to create a relatively planar surface that is suitable for the next level metallization. Multilevel **construction** is essential to the development of very large scale integration (VLSI). 2) The

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Serial No.:09/863,927

cured polyimide coatings are tough and resilient. They give excellent mechanical **protection**. 3) Polyamic acid coating **solutions** can be spun, exposed, and etched with existing equipment.

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34/3,AB/22 (Item 1 from file: 94)  
DIALOG(R) File 94:JICST-EPlus  
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03385582 JICST ACCESSION NUMBER: 97A0636760 FILE SEGMENT: JICST-E  
A Novel Positive Working Photosensitive Polymer For Semiconductor Surface  
Coating.

MAKABE H (1); BANBA T (1); HIRANO T (1)

(1) Sumitomo Bakelite Co., Ltd., Tochigi, JPN

J Photopolym Sci Technol, 1997, VOL.10,NO.2, PAGE.307-311, FIG.6, TBL.3,  
REF.5

JOURNAL NUMBER: L0202AAN

ISSN NO: 0914-9244

CODEN: JSTEE

UNIVERSAL DECIMAL CLASSIFICATION: 621.382.002.2

544.23:542.9+

LANGUAGE: English

COUNTRY OF PUBLICATION: Japan

DOCUMENT TYPE: Journal

ARTICLE TYPE: Original paper

MEDIA TYPE: Printed Publication

ABSTRACT: We developed a new positive working photosensitive polymer for semiconductor surface coating. Base resins were considered three kinds of heat-resistance polymers and we found that polybenzoxazole precursors(PBO) with photosensitizer diazonaphthoquinones and silicone modified polyamic acids added as adhesion promoters showed excellent patterning properties and film properties. Cured film of this photosensitive PBO also has not only low water absorption and low dielectric constant, but also high adhesion to substrates such as SiO<sub>2</sub>, Si<sub>3</sub>N<sub>4</sub> and molding compounds. The evaluation results of reliability made for this photosensitive PBO on testing elements was the same as that for existing non-photosensitive polyimides; it was found that the photosensitive PBO was on a practical level. (author abst.)

34/3,AB/23 (Item 1 from file: 144)  
DIALOG(R) File 144:Pascal  
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12170884 PASCAL No.: 95-0381512

Design of multilayered polymeric dielectric insulators for advanced microelectronics packaging

YOUNG TAE PARK; CHIESEL N; ECONOMY J

SASABE Hiroyuki, ed

Keimyung univ., coll. natural sci., dep. chemistry, Daegu 704-701,  
Republic of Korea

Inst. physical chemical res., Saitama 351-01, Japan

Korea-Japan joint forum 1993 organic materials for electronics and photonics (Taejon KOR) 1993-09-07

Journal: Molecular crystals and liquid crystals science and technology.  
Section A, Molecular crystals and liquid crystals, 1994, 247 351-363

Language: English

2,2-Bis(4-((4-fluorophenyl)buta-1,3-diynyl)phenoxyphenyl) hexafluoropropane and co-polymer of 1,4-bis(4-fluorophenyl)buta-1,3-diyne and hexafluorobisphenol-A were prepared for the use as photosensitive multilayered polymeric dielectric insulators. The prepared materials turned out to be stable at high temperatures as well as thermally or photochemically curable. It was found that the mechanical properties of cross-linked products by thermal or photochemical curing of the prepared diacetylenic materials were much more improved in comparison with those of cured poly(triethynylbenzene) (PTEB).

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Serial No.:09/863,927

Set	Items	Description
S1	142786	SEMICONDUCT? AND (CHIP OR CHIPS OR IC OR ICS OR INTEGRATED- (W)CIRCUIT? ? OR MICROCIRCUIT? ? OR LOGIC()CIRCUIT OR DIE? ?)
S2	6768	S1 AND DIELECTRIC?
S3	625	S2 AND (PACKAG? OR ASSEMBL?)
S4	12404	(CURING OR CURABLE OR CURE? ?) (S) (LIQUID? ? OR SOL OR SOLN OR FLUID? ? OR SOLUTION? ?)
S5	2	S3 AND S4
S6	2	RD (unique items)
S7	71109	CC=B2570 Semiconductor integrated circuits
S8	198612	S1 OR S7
S9	198612	S1 OR S8
S10	9114	S9 AND DIELECTRIC?
S11	914	S10 AND (PACKAG? OR ASSEMBL?)
S12	5	S11 AND S4
S13	3	S12 NOT S6
S14	3	RD (unique items)

01/22/2002

Serial No.:09/863,927

T S6/3,AB/1-2

>>>No matching display code(s) found in file(s): 65

6/3,AB/1 (Item 1 from file: 6)  
DIALOG(R)File 6:NTIS  
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1631886 NTIS Accession Number: AD-A245 036/9

Electronic **Packaging** Materials Science V: Symposium Held in Boston, Massachusetts on 26-29 November 1990. Materials Research Society Symposium Proceedings. Volume 203

(Monograph)

Lillie, E. D. ; Ho, P. S. ; Jaccodine, R. ; Jackson, K.

Materials Research Society, Pittsburgh, PA.

Corp. Source Codes: 085429000; 398633

Report No.: ISBN-1-55899-095-X

29 Nov 90 473p

Languages: English Document Type: Conference proceeding

Journal Announcement: GRAI9209

Materials Research Society, 9800 McKnight Road, Pittsburgh, PA 15237. HC \$42.00. No copies furnished by DTIC/NTIS.

NTIS Prices: Not available NTIS

The theme of the symposium deals with materials-related issues important to the future of technology for the **packaging** and interconnection of electronic components. This technology is on the critical path to increased performance of office computers and workstations, home computers, mainframes, supercomputers, control systems in automobiles, navigation and avionics, fast processors for medical diagnostics, or the huge telecommunications industry. It is true of all these applications that major advanced in **packaging** and interconnect are only possible with concomitant progress in materials science. Performance is not the only issue so influences, so too is compactness, lightness and cost to the consumer. The symposium included sessions on the mechanical and deformation properties of polymer interfaces (with emphasis and the effects of plastic behavior in polymeric thin films, and general attention to stress effects on reliability), protective coatings for IC 's, polymers and polymer-processing for high density **packaging** (e.g., photoimageable polyimides, use of **liquid** crystals to control thermal expansion, effect of **curing** on stress in polyimides in multilayer structures), ceramics and glass-ceramics (emphasis on aluminum nitride bulk, and interface properties), metallization techniques (low temperature CVD of copper films, laser planarization, laser assisted deposition of catalysts for electroless and electrolytic plating of copper), solders and soldering (including fatigue life predictions for solder joints), and measurement of material properties of thin films.



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6/3,AB/2 (Item 1 from file: 94)  
DIALOG(R)File 94:JICST-EPlus  
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03534563 JICST ACCESSION NUMBER: 98A0477719 FILE SEGMENT: JICST-E  
New Flip Chip Packaging System Using Non Conductive Resin Sheet

PFM-21.

ITO SATOSHI (1); MIZUTANI MASAKI (1); KUWAMURA MAKOTO (1); NORO HIROSHI (1)  
(1) Nitto Denko Corp.

Nitto Giho(Nitto Technical Report), 1998, VOL.36,NO.1, PAGE.24-29, FIG.10,  
TBL.2, REF.5

JOURNAL NUMBER: Z0901AAB ISSN NO: 0285-2462

UNIVERSAL DECIMAL CLASSIFICATION: 621.382.002.2

LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan

DOCUMENT TYPE: Journal

ARTICLE TYPE: Original paper

MEDIA TYPE: Printed Publication

ABSTRACT: A novel flip **chip packaging** technology using non-conductive resin sheet has been developed. The process flow of this new **packaging** system is as follows. First, epoxy base resin sheet is laminated onto substrate including over electrode lands. Bumped **chip** alignment and attachment has done through the resin sheet in second stage with pressure and temperature. The bumps under the **chip** penetrate with displacing the resin sheet and eventually reaching to the metal lands on the substrate. Metal connection and the sheet resin **cure** have done in the third stage. This new process has big potential to make flip **chip package** simple compared with liquid underfill flip **chip packaging** process. It is found that this new process has potential to shorten through put time drastically. The other advantages of this process are thermal stability of material in the process and warpage control performance. As thermal stability of this material, DSC peak retaining ratio of 98% can be kept for 1day at 22.DEG.C. and 3days at 25.DEG.C.. For the warpage control, as a typical result, we successfully improved thermal shock resistance performance over 10 times higher by controlling flip **chip packaging** parameters which obtains smaller warpage **package**. (author abst.)

01/22/2002

T S14/3,AB/1-3

Serial No.:09/863,927

>>>No matching display code(s) found in file(s): 65

14/3,AB/1 (Item 1 from file: 2)  
DIALOG(R)File 2:INSPEC

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6595799 INSPEC Abstract Number: B2000-06-0170J-095  
Title: Characteristics and reliability of no-flow underfills for solder  
bumped flip chip **assemblies**

Author(s): Lau, J.H.; Chang, C.; Chih-Chiang Chen

Author Affiliation: Express Packaging Syst. Inc., Palo Alto, CA, USA

Journal: International Journal of Microcircuits and Electronic Packaging  
vol.22, no.4 p.370-81

Publisher: IMAPS-Int. Microelectron. & Packaging Soc,

Publication Date: 1999 Country of Publication: USA

CODEN: IMEPES ISSN: 1063-1674

SICI: 1063-1674(1999)22:4L:370:CRFU;1-5

Material Identity Number: P802-2000-002

Language: English

Abstract: Solder bumped flip chips on low cost substrates with three different epoxy-based no-clean flux liquid-like no-flow underfills are presented in this study. This paper includes evaluation of three commercial no-flow underfills and characterization of material and process parameters. Important materials and process parameters, such as curing temperature and time, coefficient of thermal expansion, storage modulus, loss modulus, tan delta, glass transition temperature, moisture uptake, solder reflow, and post curing are discussed in this work. The curing mechanism during reflow of no-flow underfill and illustrated in this paper and a comparison of no-flow underfill and conventional underfill is also addressed. Also, cross-sections are examined for a better understanding of the effects of these no-flow underfill materials on the interconnects of the flip chip **assemblies**. Shear and thermal cycling tests and results for these flip chip **assemblies** are reported and analyzed.

Subfile: B

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Serial No.:09/863,927

14/3,AB/2 (Item 2 from file: 2)  
DIALOG(R)File 2:INSPEC

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5520653 INSPEC Abstract Number: B9704-0170J-077  
Title: Electronic and optoelectronic polymers

Author(s): Mickelson, A.R.

Author Affiliation: Guided Wave Opt. Lab., Colorado Univ., Boulder, CO,  
USA

Conference Title: Advances in Electronic Packaging 1995. Proceedings of  
the International Electronic Packaging Conference - INTERpack '95 Part  
vol.2 p.613 vol.2

Editor(s): Hsu, T.R.; Bar-Cohen, A.; Nakayama, W.  
Publisher: ASME, New York, NY, USA

Publication Date: 1995 Country of Publication: USA 2 vol. xvi+1320  
pp.

ISBN: 0 7918 1303 7 Material Identity Number: XX97-00152

Conference Title: Proceedings of INTERPACK '95. International Electronic  
Packaging Conference

Conference Sponsor: ASME; Japan Soc. Mech. Eng  
Conference Date: 26-30 March 1995

Conference Location: Lahaina, HI,  
USA

Language: English

Abstract: Summary form only given. Higher chip speeds and interconnect  
densities in electronic systems are producing a need for better  
packaging technology. Most packaging schemes use multilayer  
electrical interconnects, often placed inside a board made from polymeric  
material or a polymer dielectric stack. Epoxy laminates are cheap  
solutions, but higher clock rates need materials with better  
electrical characteristics, such as polyimides. Recent work shows that  
these materials also show favorable optical guide characteristics.  
Polyimides with additive dopants which do not compromise electrical or  
mechanical behaviour can be made into low loss waveguides, electro-optic  
switches and modulators, and possibly light amplification and generation  
devices. This is important, as there is a limit to the density with which  
one can pack electrical interconnects. Beyond the limit, lines interfere,  
ground loops carry away signal energy and ground bounce distorts signal  
fidelity. Higher speeds lead to increasing dispersion of electrical pulses,  
and further signal distortion. Although optics is not a cure-all for  
these problems, it offers designers extra freedom, especially if optical  
connections can be made in a material already used for electrical  
interconnects. This paper reviews electrical polymers, and then discusses  
the status and direction of electronics, leading to a look at optical  
properties of certain electrical polymers. We then discuss possible  
interconnect architectures using the advantages of both optical and  
electrical connections. The paper ends with discussion of future  
requirements for polymeric interconnection technology.

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Serial No.:09/863,927

14/3,AB/3 (Item 3 from file: 2)  
DIALOG(R)File 2:INSPEC  
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03523935 INSPEC Abstract Number: B90001596  
Title: Finite element analysis of TAB **packages**  
Author(s): Holalkere, V.R.  
Author Affiliation: Nat. Semicond. Corp., Santa Clara, CA, USA  
Conference Title: Proceedings of the Technical Program. NEPCON East '89  
p.762-71  
Publisher: Cahners Exposition Group, Des Plaines, IL, USA  
Publication Date: 1989 Country of Publication: USA 1028 pp.  
Conference Date: 13-15 June 1989 Conference Location: Boston, MA, USA  
Language: English

Abstract: Mechanical and electrical problems have been observed in plastic **packaged** LSI devices. Electrical parametric shifts, passivation and **dielectric** layer cracking and shifting of metallization are some of the problems which arise after plastic encapsulation and mold **cure**. Preliminary reliability tests indicated voltage shifts in the devices after mold **cure**. This was perceived to be the result of encapsulation. The obvious **solutions** to decrease the die surface stresses include using low stress mold compound as well as decoupling the die surface from plastic with a thin buffer layer of soft coatings. Finite element analysis of the die, die attach pad and plastic composite was performed with and without soft coating on the die surface. The results indicated that the die surface stresses decrease in the case of the die with soft coat. Preliminary experiments on TAB **packages** with a soft coat on the die resulted in tape shearing off of the die. This paper addresses some of the problems associated with die coating in TAB **packages**.

Set	Items	Description
S1	1400073	IC OR ICS OR INTEGRATED(W)CIRCUIT? ? OR (MICRO) (W) (CIRCUIT? ? OR CHIP? ?) OR CHIP? ? OR MICROCIRCUIT? ? OR DIE? ? OR CC=-B2570
S2	4397161	(PACKAGE? OR ENCAS????? OR PROTECT? OR CASING OR CASE OR C-AVITY OR ENCAPSULAT? OR CAPSUL?)
S3	152028	S1 AND S2
S4	2278	S3 AND ((DIELECTRIC? OR INSULAT?) (5N) (MATERIAL? ? OR ELEME-NT? ? OR LAYER? OR FILM? ? OR COAT????))
S5	0	S4 AND ((CURING OR CURABLE OR CURE OR CURED) (5N) (LIQUID? ? OR FLUID? ? OR SOL? ? OR SOLUTION? ? OR SOLN))
S6	73	S4 AND (CURING OR CURABLE OR CURE OR CURED)
S7	14	S6 AND (LIQUID? ? OR FLUID? ? OR SOL? ? OR SOLUTION? ? OR -SOLN)
S8	14	RD (unique items)
S9	9	S6 AND ((CURING OR CURABLE OR CURE OR CURED) (5N) (ELASTOMER? OR RUBBER OR POLYMER? OR PLASTIC OR THERMOPLASTIC?))
S10	8	RD (unique items)
S11	7	S10 NOT S8
S12	47	S6 AND (ELASTOMER? OR RUBBER OR POLYMER? OR PLASTIC OR THE-RMOPLASTIC?)
S13	31	S12 NOT (S8 OR S11)
S14	26	RD (unique items)
S15	6465	S1 AND (CURING OR CURABLE OR CURE OR CURED)
S16	383	S15 AND ((DIELECTRIC? OR INSULAT?) (5N) (MATERIAL? ? OR ELEM-ENT? ? OR LAYER? OR FILM? ? OR COAT????))
S17	1	S16 AND ((CURING OR CURABLE OR CURE OR CURED) (5N) (LIQUID? ? OR FLUID? ? OR SOL? ? OR SOLUTION? ? OR SOLN))
S18	1	S17 NOT (S8 OR S11 OR S14)
S19	29	S16 AND ((CURING OR CURABLE OR CURE OR CURED) (5N) (ELASTOME-R? OR RUBBER OR POLYMER? OR PLASTIC OR THERMOPLASTIC?))
S20	20	S19 NOT (S8 OR S11 OR S10 OR S14 OR S18)

01/18/2002

8/3,AB/7 (Item 1 from file: 8)  
 DIALOG(R)File 8:Ei Compendex(R)  
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02806579

E.I. Monthly No: EIM8910-035799  
 Title: Fluorinated polyimide low **dielectric coatings**.  
 Author: Ruiz, Laura M.  
 Corporate Source: Ethyl Corp, Baton Rouge, LA, USA  
 Conference Title: 3rd International SAMPE Electronics Conference:  
 Electronic Materials and Processes  
 Conference Location: Los Angeles, CA, USA Conference Date: 19890620  
 E.I. Conference No.: 12425  
 Source: International SAMPE Symposium and Exhibition v. Publ by SAMPE,  
 Covina, CA, USA. p 209-218  
 Publication Year: 1989  
 CODEN: ISSEEG ISSN: 0891-0138  
 Language: English  
 Abstract: The development of faster, more advanced integrated circuitry  
 is placing greater demands on packaging performance. One **solution** to  
 the need for increased speed is to place multiple **chips** in a single  
**package**, thereby reducing interconnect length. A critical parameter  
 in designing such packaging is the **dielectric material** chosen.  
 Much has been written about the use of standard polyimides (ave K equals  
 3.5) as dielectrics in IC fabrication. Polyimides are also being  
 evaluated and used as interlevel dielectrics in IC packaging.  
 Fluorinated polyimides can offer up to a 20% reduction in dielectric  
 constant over standard polyimides which translates to faster signal speeds  
 throughout the **package**. In addition to improved electrical  
 properties, fluorinated polyimides posses less than one-third the moisture  
 absorption of standard polyimides. This paper identifies the key  
 performance properties of fluorinated polyimides and the benefits these  
 properties bring to high speed packaging applications. Processability and  
 the effect of frequency, moisture and **cure** temperature on dielectric  
 constant are discussed. (Edited author abstract) 4 Refs.

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01/18/2002

Serial No.:09/863,927

8/3,AB/5 (Item 5 from file: 2)  
DIALOG(R)File 2:INSPEC  
(c) 2002 Institution of Electrical Engineers. All rts. reserv.

03523935 INSPEC Abstract Number: B90001596

Title: Finite element analysis of TAB packages

Author(s): Holalkere, V.R.

Author Affiliation: Nat. Semicond. Corp., Santa Clara, CA, USA

Conference Title: Proceedings of the Technical Program. NEPCON East '89  
p.762-71

Publisher: Cahners Exposition Group, Des Plaines, IL, USA

Publication Date: 1989 Country of Publication: USA 1028 pp.

Conference Date: 13-15 June 1989 Conference Location: Boston, MA, USA

Language: English

Abstract: Mechanical and electrical problems have been observed in plastic packaged LSI devices. Electrical parametric shifts, passivation and dielectric layer cracking and shifting of metallization are some of the problems which arise after plastic encapsulation and mold cure. Preliminary reliability tests indicated voltage shifts in the devices after mold cure. This was perceived to be the result of encapsulation. The obvious solutions to decrease the die surface stresses include using low stress mold compound as well as decoupling the die surface from plastic with a thin buffer layer of soft coatings. Finite element analysis of the die, die attach pad and plastic composite was performed with and without soft coating on the die surface. The results indicated that the die surface stresses decrease in the case of the die with soft coat. Preliminary experiments on TAB packages with a soft coat on the die resulted in tape shearing off of the die. This paper addresses some of the problems associated with die coating in TAB packages.

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Serial No.:09/863,927

8/3,AB/11 (Item 2 from file: 94)  
DIALOG(R)File 94:JICST-EPlus  
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03534563 JICST ACCESSION NUMBER: 98A0477719 FILE SEGMENT: JICST-E  
New Flip **chip** Packaging System Using Non Conductive Resin Sheet  
PFM-21.

ITO SATOSHI (1); MIZUTANI MASAKI (1); KUWAMURA MAKOTO (1); NORO HIROSHI (1)  
(1) Nitto Denko Corp.  
Nitto Giho(Nitto Technical Report), 1998, VOL.36,NO.1, PAGE.24-29, FIG.10,  
TBL.2, REF.5

JOURNAL NUMBER: Z0901AAB ISSN NO: 0285-2462  
UNIVERSAL DECIMAL CLASSIFICATION: 621.382.002.2  
LANGUAGE: Japanese COUNTRY OF PUBLICATION: Japan  
DOCUMENT TYPE: Journal  
ARTICLE TYPE: Original paper  
MEDIA TYPE: Printed Publication

ABSTRACT: A novel flip **chip** packaging technology using non-conductive resin sheet has been developed. The process flow of this new packaging system is as follows. First, epoxy base resin sheet is laminated onto substrate including over electrode lands. Bumped **chip** alignment and attachment has done through the resin sheet in second stage with pressure and temperature. The bumps under the **chip** penetrate with displacing the resin sheet and eventually reaching to the metal lands on the substrate. Metal connection and the sheet resin **cure** have done in the third stage. This new process has big potential to make flip **chip package** simple compared with **liquid** underfill flip **chip** packaging process. It is found that this new process has potential to shorten through put time drastically. The other advantages of this process are thermal stability of material in the process and warpage control performance. As thermal stability of this material, DSC peak retaining ratio of 98% can be kept for 1day at 22.DEG.C. and 3days at 25.DEG.C.. For the warpage control, as a typical result, we successfully improved thermal shock resistance performance over 10 times higher by controlling flip **chip** packaging parameters which obtains smaller warpage **package**. (author abst.)



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Serial No.: 09/863,927

8/3,AB/8 (Item 2 from file: 8)  
DIALOG(R) File 8: Ei Compendex(R)  
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01090607

E.I. Monthly No: EI8202012806

E.I. Yearly No: EI82051371

Title: POLYIMIDE COATINGS FOR MICROELECTRONIC APPLICATIONS.

Author: Lee, Y. K.; Craig, J. D.; Pye, W. E.

Corporate Source: DuPont, Philadelphia, Pa, USA

Source: Symp Proc - Univ, Gov, Ind, Microelectron Symp, 1981, Starkville,  
Miss, USA, May 26-28 1981 Publ by IEEE (Cat n 81CH1620-4), Piscataway, NJ,  
USA, 1981 p 10. 30-10. 39

Publication Year: 1981

Language: ENGLISH

Abstract: The use of polyimide (PI) **coatings as dielectrics** and/or for passivation for semiconductors and thin film hybrids has become increasingly important. The principal reasons are: 1) Polyamic acids, the precursors of polyimides, are solvent soluble to give viscous **liquids** that can be spun onto a wafer to create a relatively planar surface that is suitable for the next level metallization. Multilevel construction is essential to the development of very large scale integration (VLSI). 2) The **cured** polyimide coatings are tough and resilient. They give excellent **mechanical protection**. 3) Polyamic acid coating **solutions** can be spun, exposed, and etched with existing equipment.

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8/3,AB/14 (Item 2 from file: 144)

DIALOG(R)File 144:Pascal

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12103418 PASCAL No.: 95-0332898

MCM-LD: large area processing using photosensitive-BCB

STRANDJORD A J G; GARROU P E; HEISTAND R H T; TESSIER T G

Dow Chemical Co., microelectronics cent. North Carolina, Research

Triangle Park NC 27709, USA

Electronic components and technology conference, 44 (Washington DC USA)  
1994-05-01

Journal: IEEE transactions on components, packaging, and manufacturing  
technology. Part B, Advanced packaging, 1995, 18 (2) 269-276

Language: English

This paper demonstrates how laminate based printed-wiring-board technology (PWB) and thin film deposited dielectric technology (MCM-D) can be combined to form a low-cost solution for microelectronic interconnect schemes which require high density circuitry. A multilayer telecommunications module was fabricated to demonstrate the feasibility of this MCM-LD concept. Standard copper-clad laminates were processed using conventional PWB techniques to form the first level of metal interconnects (75  $\mu$ m lines and spaces). A photosensitive benzocyclobutene layer was coated onto the boards and patterned to form 50  $\mu$ m x 200  $\mu$ m nested vias down to the metal lines. A second metal interconnect layer was formed from a sputtered seed layer and plated up copper. Chip interconnection was carried out using gold wirebonding. Several large-area-processing (LAP) techniques were evaluated to determine the compatibility of the two interconnect technologies and to demonstrate the cost advantages of manufacturing large panels at high throughput levels. Spin coating, spray coating, meniscus coating, and extrusion coating were compared as dielectric deposition options and an in-line belt furnace was used to cure the dielectric layers on the laminate boards (rapid thermal curing). Laminate materials which were evaluated include: FR-4 (epoxy), BT (bismaleimide-triazine), PI (polyimide), and CE (cyanate ester)

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Serial No.:09/863,927

8/3,AB/13 (Item 1 from file: 144)  
DIALOG(R)File 144:Pascal  
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12170884 PASCAL No.: 95-0381512  
Design of multilayered polymeric dielectric insulators for advanced  
microelectronics packaging  
YOUNG TAE PARK; CHIESEL N; ECONOMY J  
SASABE Hiroyuki, ed  
Keimyung univ., coll. natural sci., dep. chemistry, Daegu 704-701,  
Republic of Korea  
Inst. physical chemical res., Saitama 351-01, Japan  
Korea-Japan joint forum 1993 organic materials for electronics and  
photonics (Taejon KOR) 1993-09-07  
Journal: Molecular crystals and liquid crystals science and technology.  
Section A, Molecular crystals and liquid crystals, 1994, 247 351-363  
Language: English  
2,2-Bis(4-((4-fluorophenyl)buta-1,3-diynyl)phenyloxyphenyl) hexafluoropro  
pane and co-polymer of 1,4-bis(4-fluorophenyl)buta-1,3-diyne and  
hexafluorobisphenol-A were prepared for the use as photosensitive  
multilayered polymeric **dielectric insulators**. The prepared  
**materials** turned out to be stable at high temperatures as well as  
thermally or photochemically **curable**. It was found that the  
mechanical properties of cross-linked products by thermal or photochemical  
**curing** of the prepared diacetylenic materials were much more improved  
in comparison with those of **cured** poly(triethynylbenzene) (PTEB).

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Serial No.:09/863,927

11/3,AB/4 (Item 4 from file: 2)  
DIALOG(R)File 2:INSPEC  
(c) 2002 Institution of Electrical Engineers. All rts. reserv.

5932657 INSPEC Abstract Number: B9807-0560-007

Title: Thermal characterization of thin polymer films using a surface acoustic wave sensor

Author(s): Mileham, R.D.; Sternhagen, J.D.; Galipeau, D.W.

Author Affiliation: Dept. of Electr. Eng., South Dakota State Univ., Brookings, SD, USA

Conference Title: Proceedings. 1997 International Symposium on Microelectronics (SPIE vol.3235) p.226-31

Publisher: IMAPS - Int. Microelectron. & Packaging Soc, Reston, VA, USA

Publication Date: 1997 Country of Publication: USA xvii+707 pp.

ISBN: 0 930815 50 5 Material Identity Number: XX98-00801

Conference Title: Proceedings 1997 International Symposium on Microelectronics

Conference Sponsor: IMAPS - Int. Microelectron. & Packaging Soc

Conference Date: 14-16 Oct. 1997 Conference Location: Philadelphia, PA, USA

Language: English

Abstract: Applications of polymer films in microelectronics have increased rapidly in recent years. These applications include inter-metal dielectrics in **integrated circuits**, flexible and multilayer substrates, encapsulants, and as photoresists. These applications have resulted in the need for new film characterization methods since these films are much thinner than those used previously. In particular, there is a need to study glass transition, viscoelasticity and mass loss during **curing** of new high temperature **polymer** films. A high temperature thermal characterization system for thin polymer films based on a surface acoustic wave sensor was developed that could operate up to 400 degrees C. Sensor heaters examined included thick film on alumina and etched foil. It was found that polymer viscoelastic properties could be measured, including the temperature of first and second film resonance points. Gravimetric studies were inconclusive due to the much larger viscoelastic response. The etched foil heater could operate up to a temperature of 500 degrees C versus 320 degrees C for the thick film heater.

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Serial No.:09/863,927

14/3,AB/3 (Item 3 from file: 2)  
DIALOG(R)File 2:INSPEC  
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6491892 INSPEC Abstract Number: B2000-03-2250-009

Title: Reducing polyimide **cure** time for MCM-D

Author(s): Wilkins, W.; Schuckert, C.

Author Affiliation: New Technol. Lab., Union Semicond. Technol. Corp.,  
Chippewa Falls, WI, USA

Journal: Advanced Packaging vol.8, no.10 p.42-6

Publisher: IHS Publishing Group,

Publication Date: Nov.-Dec. 1999 Country of Publication: USA

CODEN: ADPAFZ ISSN: 1065-0555

SICI: 1065-0555(199911/12)8:10L:42:RPCT;1-M

Material Identity Number: F109-2000-001

U.S. Copyright Clearance Center Code: 1065-0555/99/\$1.00+.50

Language: English

Abstract: Polyimides are commonly used as both inner layer dielectrics and as the solder dam in the fabrication of multichip module deposited dielectric (MCM-D) **packages**. The New Technology Laboratory (NTL) used PI-2611 polyimide as a thin film dielectric to make MCMs. This **polymer** was chosen for its low-stress properties, high modulus and close coefficient of thermal expansion match to silicon. However, the **cure** cycle that was initially implemented into production was very long. As production volumes increased, it became desirable to shorten the **curing** process. This article reviews the following: MCM product applications; PI-2611 polyimide and its applicability in the fabrication of thin film multilayer **packages**; the experimental design to test the shortened polyimide **cure** cycles; and the resulting effects on stress, adhesion and dielectric constant.

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Serial No.:09/863,927

14/3,AB/8 (Item 8 from file: 2)  
DIALOG(R)File 2:INSPEC  
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04093458 INSPEC Abstract Number: A9207-8235-001

Title: Effects of process history and aging on the properties of polyimide films

Author(s): Denton, D.D.; Buncick, M.C.; Pranjoto, H.

Author Affiliation: Dept. of Electr. & Computer Eng., Wisconsin Univ.,  
Madison, WI, USA

Journal: Journal of Materials Research vol.6, no.12 p.2747-54

Publication Date: Dec. 1991 Country of Publication: USA

CODEN: JMRREE ISSN: 0884-2914

Language: English

Abstract: Polyimide is used extensively in a variety of **integrated circuit** packaging applications. It is a good **dielectric material** with excellent planarizing capabilities, but like most **polymers**, it absorbs moisture. This hygroscopic behavior can lead to reliability problems in **integrated circuit packages**. The effects of variations in process history on moisture uptake are examined using gravimetric measurement techniques. In particular, the effects of **cure** schedule and exposure to high temperature/high humidity environments (85 degrees C/85% RH) on steady state moisture uptake are reported. Steady state moisture uptake is shown to be a decreasing function of **cure** temperature. Samples **cured** at 250 degrees C absorb 25% more moisture by weight than do samples **cured** at 400 degrees C. Moreover, the steady state moisture uptake in polyimide is greater after the samples have been 'aged' in a high temperature and humidity ambient. The bulk and surface chemical composition are also monitored as a function of aging using Fourier transform infrared spectroscopy (FTIR) and electron spectroscopy for chemical analysis (ESCA), respectively. The PI surface chemistry degrades after 700 h in an 85 degrees C/85% RH environment. The bulk chemical composition appears to be unaffected.

01/18/2002

14/3,AB/6 (Item 6 from file: 2)  
 DIALOG(R)File 2:INSPEC  
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4823423 INSPEC Abstract Number: B9412-0170J-067  
 Title: Development of a cost effective high performance metal QFP

packaging system

Author(s): Mahulikar, D.; Pasqualoni, A.; Crane, J.; Braden, J.  
 Author Affiliation: Metals Res. Labs., Olin Corp., New Haven, CT, USA

p.405-11

Publisher: IEEE, New York, NY, USA

Publication Date: 1993 Country of Publication: USA xvii+1166 pp.

ISBN: 0 7803 0794 1

U.S. Copyright Clearance Center Code: 0569-5503/93/0000-0405\$3.00

Conference Title: Proceedings of IEEE 43rd Electronic Components and Technology Conference (ECTC '93)

Conference Date: 1-4 June 1993 Conference Location: Orlando, FL, USA

Language: English

Abstract: This paper describes the design and development of MQAD technology. The MQAD packaging system is a high performance reliable technology currently in use for packaging of microprocessors, high-speed ASIC devices, including CMOS, Bi CMOS, Bi polar, gallium arsenide, and other high performance IC's. The packaging technology is being used for devices dissipating up to 14 watts and switching speed of up to 300 MHz. The design and development was carried out with the objectives of high thermal performance (up to 15 watts), high electrical performance (inductance and capacitances lower than comparable PQFPs) and reliability superior to the PQFPs. The approach taken was; to use an adhesively bonded metal **package**. An aluminum alloy lid and base were chosen to give excellent heat dissipation ability, mechanical integrity and light weight construction. A special anodization process was developed to put a hard, electrically **insulating** black colored anodic **film** on the aluminum alloy components. The adhesive seal is a filled epoxy having low dielectric constant and low ionic content and with excellent adhesion to both copper alloys and aluminum anodic films, especially in moist environments. The leadframe chosen is a high-strength, thermally conductive copper alloy. The assembly process for the MQAD **package** emulates the PQFP assembly process except that the molding step is replaced by a single step pad attach simultaneous with the seal adhesive lamination/cure process. The leadframe pad is attached to the anodized aluminum alloy base via a silver-filled epoxy paste. The **package** was thoroughly tested for reliability and fully characterized for thermal and electrical performance. Reliability tests performed include temperature cycling, thermal shocks, solvent resistance, flammability, pressure cooker, and vapor phase shocks. Reliability of MQAD **packages** is superior to that of PQFPs. Characterization includes  $\theta_{ja}$  and  $\theta_{jc}$ , and resistance, inductance and capacitance measurements. Thermal and electrical performance of MQAD **packages** equal or exceed that of comparable plastic or ceramic QFPs. The high reliability and performance of MQAD was confirmed by many customers and users and has been published. Because of these benefits, the technology is being further extended to advanced **packages** such as MCMS, TAB and ball or pad grid arrays.

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14/3,AB/12 (Item 12 from file: 2)  
DIALOG(R)File 2:INSPEC  
(c) 2002 Institution of Electrical Engineers. All rts. reserv.

02160058 INSPEC Abstract Number: B84000158

Title: Individual **encapsulation** for **integrated circuits**:  
how to use thermal analysis to optimize **curing** conditions towards  
reliability

Author(s): Baudry, H.; Kersuzan, G.

Author Affiliation: LEP, Limeil-Brevannes, France

Conference Title: Proceedings of the 4th European Hybrid Microelectronics  
Conference p.111-21

Publisher: DIS Congress Service, Vanlose/Copenhagen, Denmark

Publication Date: 1983 Country of Publication: Denmark xv+563 pp.

Conference Date: 18-20 May 1983 Conference Location: Copenhagen,  
Denmark

Language: English

Abstract: Shows, using a commercial epoxy encapsulant (HYSOL ES 4228)  
chosen as an example, how thermal analysis allows to determine a good  
incoming inspection of the different purchased batches, to fix the best  
**curing** conditions and to control the manufacturing process. Starting  
from **curing** conditions (temperature, atmosphere...) determined by the  
experiments described, C-MOS ICs of a given type known to be very  
surface sensitive to the environment, have been **encapsulated**. The  
reliability of such a **protection** is tested under severe experimental  
conditions.



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Serial No.:09/863,927

14/3,AB/11 (Item 11 from file: 2)

DIALOG(R)File 2:INSPEC

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03238611 INSPEC Abstract Number: B88064146

Title: New systems for fabrication of wafer scale interconnections in multichip **packages**

Author(s): McDonald, J.F.; Lin, H.T.; Majid, N.; Greub, H.; Philhower, R.; Dabral, S.

Author Affiliation: Center for Integrated Electron., Rensselaer Polytech. Inst., Troy, NJ, USA

Conference Title: 1988 Proceedings of the 38th Electronics Components Conference (88CH2600-5) p.305-14

Publisher: IEEE, New York, NY, USA

Publication Date: 1988 Country of Publication: USA x+664 pp.

U.S. Copyright Clearance Center Code: 0569-5503/88/0000-0305\$01.00

Conference Sponsor: IEEE; Electron. Ind. Assoc

Conference Date: 9-11 May 1988 Conference Location: Los Angeles, CA, USA

Language: English

Abstract: Processing tools for improving the yield in the fabrication of wafer-scale interconnections for multichip **packages** are discussed. Tools for deposition and etching of dielectrics and for metal deposition are covered. Efforts to introduce parylene **dielectric films**, which have lower **curing** temperatures than polyimide, are discussed. The need to avoid high-temperature processing steps in metal film production is stressed. The use of focused electron and ion beam repair strategies to cope with residual faults in a high-yield WSI lift-off process is explored.

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Serial No.:09/863,927

14/3,AB/10 (Item 10 from file: 2)  
DIALOG(R)File 2:INSPEC

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03743148 INSPEC Abstract Number: B90068414

Title: Gravimetric measurements of moisture uptake in polyimide films used in **integrated circuit** packaging

Author(s): Denton, D.D.; Pranjoto, H.

Author Affiliation: Dept. of Electr. & Comput. Eng., Wisconsin Univ., Madison, WI, USA

Conference Title: Electronic Packaging Materials Science IV. Symposium p.97-105

Editor(s): Jaccodine, R.; Jackson, K.A.; Lillie, E.D.; Sundahl, R.C.  
Publisher: Mater. Res. Soc, Pittsburgh, PA, USA

Publication Date: 1989 Country of Publication: USA xiii+494 pp.

Conference Sponsor: Army Res. Office; Allied-Signal Corp.; Amoco; Dow; Intel; Office Naval Res

Conference Date: 24-28 April 1989 Conference Location: San Diego, CA, USA

Language: English

Abstract: Polyimide is used extensively in a variety of **integrated circuit** packaging applications. It is a good **dielectric material** with excellent planarizing capabilities, but like most **polymers**, it absorbs moisture. This hygroscopic behavior can lead to reliability problems in **integrated circuit packages**. The effects of variations in process history on moisture uptake are examined using gravimetric measurement techniques. In particular, the effects of **cure** schedule and exposure to high temperature/high humidity environments on steady state moisture uptake are reported. Steady state moisture uptake is shown to be a decreasing function of **cure** temperature. Moreover, the steady state moisture uptake in polyimide is greater after the samples have been 'aged' in a high temperature and humidity ambient. Electrical measurements are used to examine the effects of **cure** temperature on diffusion kinetics of moisture in polyimide. The diffusion coefficient decreases with increasing **cure** temperature.

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Serial No.:09/863,927

14/3,AB/9 (Item 9 from file: 2)  
DIALOG(R)File 2:INSPEC  
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03743173 INSPEC Abstract Number: B90068418

Title: Photosensitive polyimides

Author(s): Hiramoto, H.

Author Affiliation: Electron. & Imaging Mater. Res. Labs., Toray Ind.  
Inc., Japan  
Conference Title: Advanced Electronic Packaging Materials. Symposium  
p.87-97

Editor(s): Barfknecht, A.T.; Partridge, J.P.; Chen, C.J.; Che-Yu Li  
Publisher: Mater. Res. Soc, Pittsburgh, PA, USA

Publication Date: 1990 Country of Publication: USA xi+380 pp.

Conference Date: 27-29 Nov. 1989 Conference Location: Boston, MA, USA

Language: English

Abstract: Photosensitive polyimides are used as insulation and protection layers for microelectronics. They can easily give fine-patterned films with excellent characteristics of polyimides by photolithographic procedure. Photosensitive groups, such as double bonds, azides, o-nitrobenzyl and o-naphthoquinonediazides, are incorporated to polymer chains through covalent bonds or acid-base ion bonds. Characteristics of photosensitive polyimides are determined by two factors, the way of introducing photosensitive groups and the structures of polyimide backbone chains. Photosensitivity, resolution, purity and imidization mainly depends on the former factor. The film properties after curing are mainly determined by the latter. The film properties, however, are affected by the former when imide cyclization is imperfect. Photosensitive polyimides are widely used a protection and insulation layers of VLSI, multi-chip modules for computers, telecommunication, linephotosensors, thermal-heads, etc.

01/18/2002

Serial No.: 09/863,927

14/3,AB/15 (Item 1 from file: 8)  
DIALOG(R) File 8: Ei Compendex(R)  
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05930917

E.I. No: EIP01446711009

Title: Process for fabricating dense, **chips**-first MCMs with thinned  
**die**

Author: LeBlanc, J.J.; Tumminelli, R.P.; Singleton, M.C.; Ayers, B.P.;  
Haley, J.F.; Ives, G.V.; Dineen, A.D.

Corporate Source: The Charles Stark Draper Lab., Inc. Electron. Packaging  
Prototyping Div., Cambridge, MA 02139, United States

Conference Title: 2001 HD Interntional Conference on Hig-Density  
Interconnect and Systems Packaging

Conference Location: Santa Clara, CA, United States Conference Date:  
20010417-20010420

E.I. Conference No.: 58644

Source: Proceedings of SPIE - The International Society for Optical  
Engineering v 4428 2001. p 364-368

Publication Year: 2001

CODEN: PSISDG ISSN: 0277-786X

Language: English

Abstract: There is a continual push in the microelectronic industry for denser packaging both in footprint area and total volume. We present a robust process for fabricating **chips** first multi-**chip** modules (MCMs). The process incorporates the use of **die** that are thinned to six mils and subsequently placed to within 130mum (0.005 double prime ) of each other. The placement accuracy is +/-13mum (0.0005 double prime ) and can be maintained through **curing**. This allows us to use fixed drill files and masks with 75mum (0.003 double prime ) capture pads. The six mil **die** are surrounded with a polyimide windowpane to create a planar surface on which to construct the interconnect. A polyimide **dielectric layer** is then laminated on top of the **die**, blind vias are laser drilled to the **die**, and a Ti/Cu/Ti interconnect structure is then built over the **die**. Subsequent layers are then built up, with the interconnect residing above the **die**. When modules are diced out, the overall area is only slightly larger than the combined area of the **die**. Total module thickness for a four level module is typically 560mum (0.022 double prime ). We also will present thermal shock data for our interconnect structure. 5 Refs.

01/18/2002

Serial No.:09/863,927

14/3,AB/13 (Item 13 from file: 2)  
DIALOG(R)File 2:INSPEC  
(c) 2002 Institution of Electrical Engineers. All rts. reserv.

00991286 INSPEC Abstract Number: B77000506  
Title: **Encapsulation of integrated circuits** containing  
beam leaded devices with a silicone RTV dispersion  
Author(s): Jaffe, D.  
Author Affiliation: Bell Labs., Allentown, PA, USA  
Journal: IEEE Transactions on Parts, Hybrids and Packaging vol.PHP-12,  
no.13 p.182-7  
Publication Date: Sept. 1976 Country of Publication: USA  
CODEN: IEPHAA ISSN: 0361-1000  
Conference Title: 26th Electronic Components Conference  
Conference Date: 26-28 April 1976 Conference Location: San Francisco,  
CA, USA

Language: English

Abstract: Reviews the results of a number of investigations performed to evaluate the use of an RTV silicone **rubber** dispersion for the **encapsulation** (conformal coating) of the **integrated circuits** containing beam leaded silicon **integrated circuit** (SIC) devices. The dispersion consists of approximately 67% xylene and 33% solids by weight. The investigations described include: measurement techniques for and typical values of the properties of the as-received dispersion and of the material after **curing**; the determination of the suitability of the dispersion to be applied to **integrated circuits** containing SIC's by a flow coat technique, and of its capability to completely fill under SIC's after **curing**; and the performance of **encapsulated** test specimens and circuits in some initial accelerated bias-humidity and temperature cycling tests. In addition, several other factors relevant to determining the suitability of the dispersion for particular circuit applications are briefly discussed.

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Serial No.: 09/863,927

14/3,AB/12 (Item 12 from file: 2)  
DIALOG(R) File 2:INSPEC

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02160058 INSPEC Abstract Number: B84000158

Title: Individual **encapsulation** for **integrated circuits**:  
how to use thermal analysis to optimize curing conditions towards  
reliability

Author(s): Baudry, H.; Kersuzan, G.

Author Affiliation: LEP, Limeil-Brevannes, France

Conference Title: Proceedings of the 4th European Hybrid Microelectronics  
Conference p.111-21

Publisher: DIS Congress Service, Vanlose/Copenhagen, Denmark

Publication Date: 1983 Country of Publication: Denmark xv+563 pp.

Conference Date: 18-20 May 1983 Conference Location: Copenhagen,  
Denmark

Language: English

Abstract: Shows, using a commercial epoxy encapsulant (HYSOL ES 4228)  
chosen as an example, how thermal analysis allows to determine a good  
incoming inspection of the different purchased batches, to fix the best  
curing conditions and to control the manufacturing process. Starting  
from curing conditions (temperature, atmosphere...) determined by the  
experiments described, C-MOS ICs of a given type known to be very  
surface sensitive to the environment, have been **encapsulated**. The  
reliability of such a **protection** is tested under severe experimental  
conditions.

01/18/2002

Serial No.:09/863,927

14/3,AB/19 (Item 5 from file: 8)  
DIALOG(R)File 8: Ei Compendex(R)  
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04669618

E.I. No: EIP97043621866  
Title: Embedding technology - a **chip**-first approach using BCB  
Author: Toepper, M.; Buschick, K.; Wolf, J.; Glaw, V.; Hahn, R.; Dabek, A.; Ehrmann, O.; Reichl, H.  
Corporate Source: Technical Univ of Berlin, Berlin, Ger  
Conference Title: Proceedings of the 1997 3rd International Symposium and Exhibition on Advanced Packaging Materials Processes, Properties and Interfaces  
Conference Location: Braselton, GA, USA Conference Date: 19970309-19970312

E.I. Conference No.: 46261  
Source: Proceedings of the International Symposium and Exhibition on Advanced Packaging Materials Processes, Properties and Interfaces 1997. p 11-14

Publication Year: 1997

CODEN: 002572

Language: English

Abstract: With the current trend to ever faster clock rates the propagation delays between the **chips** constitute a significant portion of the clock cycle. Mounting both active and passive devices as closely together as possible will therefore boost system's performance. Although flip-chipped devices have good performance, design constraints may prevent the placement of pads to comply with flip **chip** design rules. An additional advantage of the embedding technology is the possibility to employ 3-D stacking, the highest **package** density. Bare dice and standard passive components were embedded into a ceramic substrate to achieve a common, planar surface. Hence by employing the thinfilm processing all components can be directly interconnected to the copper routing of the module. Benzocyclobutene (BCB) with its low **curing** temperature is preferred as dielectrical **polymer** for the embedding technology. Application of bonding or soldering techniques which might limit the reliability is avoided. This offers excellent electrical properties of the wiring system. By planarizing the reverse side of the MCM a low thermal resistance between heat sink and dice can be accomplished simultaneously for all embedded components. An SRAM MCM and a Thermotest MCM demonstrate the facility of the embedding technology. (Author abstract)  
5 Refs.

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Serial No.:09/863,927

20/3,AB/14 (Item 14 from file: 2)  
DIALOG(R)File 2:INSPEC  
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01445553 INSPEC Abstract Number: B80003554

Title: Method for improving adhesion of polyimides

Author(s): Abrahmovich, K.M.; Gleason, R.T.; Motsiff, W.T.

Author Affiliation: IBM Corp., Armonk, NY, USA

Journal: IBM Technical Disclosure Bulletin vol.22, no.1 p.42

Publication Date: June 1979 Country of Publication: USA

CODEN: IBMTAA ISSN: 0018-8689

Language: English

Abstract: Multiple layers of **cured** polyamide polymers when used as insulators in **integrated circuit** applications normally show a low degree of adhesion to each other. This method provides improved adhesion between contacting layers. The **cured** polyimide film is exposed to an aqueous solution of tetra-alkyl ammonium hydroxide salt, rinsed in water, and exposed to a dilute aqueous solution of acetic acid, followed by a second water rinse. The wafer is then spun dry and a second layer is applied and **cured**. This method is believed to form a chemical rather than a physical bond.



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20/3,AB/18 (Item 4 from file: 8)  
DIALOG(R) File 8: Ei Compendex(R)  
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02523856

E.I. Monthly No: EIM8801-003835

Title: HIGH-DENSITY MULTILAYER HYBRID CIRCUITS MADE WITH POLYMER  
INSULATING LAYERS (POLYHIC'S).

Author: Shiflett, C. C.; Buchholz, D. B.; Faudskar, C. C.; Small, R. D.;  
Markham, J. L.

Corporate Source: AT&T Bell Lab

Conference Title: Proceedings of the 1986 International Symposium on  
Microelectronics.

Conference Location: Atlanta, GA, USA Conference Date: 19861006  
E.I. Conference No.: 10579

Source: Publ by Int Soc for Hybrid Microelectronics, Reston, VA, USA p  
481-486

Publication Year: 1986

ISBN: 0-930815-16-5

Language: English

Abstract: An extension of the Hybrid Integrated Circuit  
technology, designated POLYHIC's, has been developed by adding alternate  
layers of polymer and metal to conventional Hybrid Integrated  
Circuits. The polymer formulation was developed within AT&T to  
provide the required combination of lithographic, thermal, and mechanical  
properties. The cured polymer has a glass transition  
temperature of about 150 DEGREE C, and will withstand soldering  
temperatures without damage. The dielectric constant of 3.6 and a polymer  
thickness of 50 micrometers allows fabrication of controlled impedance  
lines. The multiple layers of circuitry produce high packing densities and  
simplify circuit layout because of the high interconnectability of the  
structure. Design rules and fabrication procedures have been developed.  
Accelerated environmental tests have been performed, including  
temperature-humidity-bias, elevated temperature, and temperature cycling. 3  
refs.

01/18/2002

Serial No.:09/863,927

20/3,AB/16 (Item 2 from file: 8)  
DIALOG(R)File 8:Ei Compendex(R)  
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05259924

E.I. No: EIP99034624765

Title: Design of coplanar waveguide multilayer square spiral inductors  
for monolithic microwave **integrated circuits**

Author: Budimir, Djuradj; Robertson, Ian D.; Wang, Q.H.; Rezazadeh, A.A.  
Corporate Source: Univ of Westminster, London, UK

Source: International Journal of RF and Microwave Computer-Aided  
Engineering v 9 n 2 Mar 1999. p 86-92

Publication Year: 1999

CODEN: IJMEFQ ISSN: 1096-4290

Language: English

Abstract: A square indicator using multilayer coplanar waveguide  
transmission lines on a GaAs fabricated by using monolithic microwave  
**integrated circuits** (MMIC) technology is presented. The  
polyimide layer formation, **curing** and dry etching processes are used  
in an attempt to obtain high quality **dielectric layers** suitable  
for MMIC applications. The experimental fabrication progress provides two  
metal **layers** with two polyimide spacer **dielectric layers**.  
A brief overview of the electromagnetic design process is included. The  
performance of the proposed spiral inductor is investigated experimentally  
and with electromagnetic simulations (Sonnet em) up to 20 GHz using  
RF-on-water measurements. A very good agreement is achieved, despite the  
highly three-dimensional nature of the structure. (Author abstract) 22  
Refs.

L1 579001 SEA FILE=WPIX ABB=ON PLU=ON H01L?/IC  
 L2 89905 SEA FILE=WPIX ABB=ON PLU=ON SEMICONDUCT? AND (CHIP OR IC OR  
 INTEGRATED CIRCUIT OR MICROCIRCUIT OR LOGIC CIRCUIT)  
 L3 70939 SEA FILE=WPIX ABB=ON PLU=ON L1 AND L2  
 L4 47928 SEA FILE=WPIX ABB=ON PLU=ON H01L021?/IC AND L3  
 L5 3027 SEA FILE=WPIX ABB=ON PLU=ON DIELECTRIC? AND L4  
 L6 186 SEA FILE=WPIX ABB=ON PLU=ON (PACKAG? OR ASSEMBL?) AND L5  
 L7 22037 SEA FILE=WPIX ABB=ON PLU=ON (CURING OR CURABLE OR CURE#) (S)  
 (LIQUID OR SOLUTION)  
 L8 7 SEA FILE=WPIX ABB=ON PLU=ON L6 AND L7

=> D MAX 1-

YOU HAVE REQUESTED DATA FROM 7 ANSWERS - CONTINUE? Y/(N):y

L8 ANSWER 1 OF 7 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD  
 AN 2001-234558 [24] WPIX  
 CR 2000-685985 [60]  
 DNN N2001-167720 DNC C2001-070163  
 TI Encapsulating microelectronic **assembly** involves formation of  
**cured** supported barrier layer before applying **curable**  
**liquid** encapsulant to **assembly**.  
 DC A85 L03 U11  
 IN FJELSTAD, J; SMITH, J W  
 PA (TESS-N) TESSERA INC  
 CYC 1  
 PI US 6204091 B1 20010320 (200124)\* 13p H01L023-34 <--  
 ADT US 6204091 B1 Provisional US 1996-32871P 19961213, Cont of US 1997-984933  
 19971204, US 2000-505609 20000217  
 PRAI US 1996-32871P 19961213; US 1997-984933 19971204; US 2000-505609  
 20000217  
 IC ICM H01L023-34  
 ICS H01L021-44; H01L021-48; H01L021-50;  
 H01L023-48  
 AB US 6204091 B UPAB: 20010502  
 NOVELTY - A microelectronic **assembly** is encapsulated by forming  
 a **curable** barrier layer on a support; **assembling** the  
 supported barrier layer and microelectronic **assembly**;  
**curing** the barrier layer; applying a **curable**  
**liquid** encapsulant to the **assembly**; and **curing**  
 the encapsulant. The barrier layer has openings that are patterned  
 corresponding to the terminals of the **assembly**.  
 DETAILED DESCRIPTION - Encapsulating a microelectronic  
**assembly** comprises providing at least one microelectronic  
**assembly** having microelectronic elements (12, 14) that define  
 exterior surfaces and bond windows. The **assembly** also includes  
 an array of terminals (24) which are exposed at the exterior surfaces. A  
 layer of **liquid curable** barrier material (32) is  
 provided on a support (36). This barrier layer has openings (38) that are  
 patterned corresponding to the terminal array. The support and the  
 microelectronic elements are **assembled** so that the barrier layer  
 contacts the exterior surfaces and covers the bond windows. The openings  
 in the barrier layer are aligned with the terminals. The barrier material  
 is **cured** while it is in contact with exterior surfaces and the  
 support. After **curing**, a **curable liquid**  
 encapsulant (40) is applied to the **assembly**, and **cured**  
 . The barrier layer prevents the encapsulant to flow through the bond  
 windows. An INDEPENDENT CLAIM is also included for a microelectronic  
**assembly** obtained by the above-mentioned method.  
 USE - For encapsulating a microelectronic **assembly**, e.g.  
 semiconductor chip package.  
 ADVANTAGE - The inventive method provides controlled encapsulation of  
 the microelectronic **assembly** without contaminating the terminals  
 of the **assembly**.

DESCRIPTION OF DRAWING(S) - The figure illustrates the encapsulation of the microelectronic **assembly**.

**Semiconductor chip** 12

**Dielectric sheet** 14

Terminals 24

Compliant layer 30

Barrier Layer 32

Support 36

Openings 38

Liquid encapsulant 40

Dwg.1E/5

TECH US 6204091 B1 UPTX: 20010502

TECHNOLOGY FOCUS - POLYMERS - Preferred Material: The **curable liquid** encapsulant is silicone elastomer, flexibilized epoxy, or gel.

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Component: The barrier layer is a **dielectric** material. The microelectronic elements consist of first and second microelectronic elements consisting of a **semiconductor chip** and a flexible **dielectric** sheet, respectively. A compliant layer (30) is **assembled** between the **chip** and the **dielectric** sheet. The support maybe a flexible storage liner.

FS CPI EPI

FA AB; GI

MC CPI: A99-A; L04-C20; L04-C20A

EPI: U11-D02B; U11-D03A

L8 ANSWER 2 OF 7 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD

AN 2000-685985 [67] WPIX

DNN N2000-507093 DNC C2000-208615

TI Encapsulation of microelectronic **assembly** involves curing a barrier layer while in contact with exterior surfaces to form a layer that will cover apertures.

DC A32 A85 L03 U11 U14

IN FJELSTAD, J; SMITH, J W

PA (TESS-N) TESSERA INC

CYC 1

PI US 6130116 A 20001010 (200067)\* 13p H01L021-56 <--

ADT US 6130116 A Provisional US 1996-32871P 19961213, US 1997-984933 19971204

PRAI US 1996-32871P 19961213; US 1997-984933 19971204

IC ICM H01L021-56

AB US 6130116 A UPAB: 20010502

NOVELTY - A microelectronic **assembly** (30) is encapsulated by **curing** a barrier layer (32) on a supporting element (36) to form a layer that will cover the apertures, applying a **curable liquid** encapsulant (40) to the microelectronic **assemblies**, and **curing** the encapsulant. The barrier layer maintains in contact with the exterior surface (22) as **curing** process occurs.

DETAILED DESCRIPTION - Encapsulating a microelectronic **assembly** comprises:

- (a) providing microelectronic **assemblies** having elements (12, 14) e.g. **semiconductor chip** and flexible **dielectric** sheet which defines exterior surfaces and an array of terminals (24) exposed at the exterior surfaces;
- (b) providing a barrier layer on a supporting element;
- (c) **assembling** the supporting element and the microelectronic elements for the layer to contact to the exterior surfaces and to cover apertures;
- (d) curing the barrier layer while maintaining the barrier layer in contact with the exterior surfaces to form a layer which covers the apertures;
- (e) applying a **curable liquid** encapsulant to the microelectronic **assemblies**; and

(f) curing the encapsulant.

The microelectronic elements define apertures through the exterior surfaces. The barrier layer has openings (38) aligned to the terminals. The layer on a surface of the supporting element is provided by screen-printing.

USE - The method is used for encapsulating a microelectronic assembly.

ADVANTAGE - The encapsulation method provides no contaminants at the terminals located on a surface of a **semiconductor chip**. It also provides the formation of an efficacious compliant layer between the microelectronic elements. The wet barrier layer is better able to conform to the contour of the exterior surfaces because it is pliable prior to curing. Hence no gaps formed between the barrier layer and the exterior surfaces.

DESCRIPTION OF DRAWING(S) - The figure shows further stages of a method of encapsulating a microelectronic **assembly**.

Microelectronic **assemblies** having elements 12, 14

Exterior surface 22

Terminals 24

Microelectronic **assembly** 30

Barrier layer 32

Supporting element 36

Openings 38

Encapsulant 40

Dwg.1E/5

TECH US 6130116 A UPTX: 20001223

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Method: The microelectronic **assemblies** are stored after curing the encapsulant. During storage, the cured barrier layer and the supporting element cooperatively surround to protect the terminals from contaminants. The supporting elements are removed from the barrier layer for the openings to be accessible through the openings. The terminals are electrically connected to conductive metallic materials on an external circuit element e.g. printed circuit board. The microelectronic **assemblies** interconnect with the external circuit element. The supporting element is removed at less than 24 hours before the **assemblies** are connected to the external circuit element. The supporting element is dissolved in water.

TECHNOLOGY FOCUS - POLYMERS - Preferred Method: The method further includes providing an adhesive between the barrier layer and the exterior surfaces before the **assembling** step.

FS CPI EPI

FA AB; GI

MC CPI: A11-B05; A11-C02C; A12-E04; A12-E07C; L04-C20A

EPI: U11-D01A5; U11-D01A7; U11-E02A1; U14-H03A4B

PLE UPA 20010502

[1.1] 018; P0000; L9999 L2391; L9999 L2073; M9999 M2073; S9999 S1434

[1.2] 018; ND01; ND07; N9999 N7170 N7023; Q9999 Q7523; Q9999 Q7374-R  
Q7330; Q9999 Q7476 Q7330; K9416; Q9999 Q6644-R; Q9999 Q9154

L8 ANSWER 3 OF 7 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD

AN 2000-327690 [28] WPIX

CR 1999-370609 [31]

DNN N2000-246563 DNC C2000-099244

TI Resilient element for forming a compliant interface between **semiconductor chip** and other microelectronic element comprises fibrous intermediary layers in elastomeric binder which are wettable by snap-curing adhesive.

DC A85 L03 U11

IN DISTEFANO, T H; KOVAC, Z; SMITH, J W

PA (TESS-N) TESSERA INC

CYC 1

PI US 6030856 A 20000229 (200028)\* 18p H01L021-44 <--

ADT US 6030856 A Provisional US 1996-19475P 19960610, US 1997-872379 19970610  
PRAI US 1996-19475P 19960610; US 1997-872379 19970610

IC ICM H01L021-44

ICS H01L021-48; H01L021-50

AB US 6030856 A UPAB: 20000613

NOVELTY - Microelectronic **package** is made by **assembling** next to a microelectronic element a resilient element having fibrous intermediary layers, which can be wetted by adhesive. A second microelectronic element is placed next to the resilient element and adhesive is cured while in contact with at least one intermediary layers and the microelectronic elements. Electrically conductive parts of the two elements are connected together after curing the adhesive.

DETAILED DESCRIPTION - Preferred Features: The fibrous material of the intermediary layers includes fibers protruding from the layers. The fibers are cellulose, cotton, or polypropylene or nylon synthetic fibers and the material may be in the form of paper or woven or non-woven fabric. The adhesive intermeshes with the fibers after **curing** and is in contact with voids in the layers. The resilient element also has cells remote from the voids. The adhesive is **cured** by applying energy to cause it to change from one solid state to a second solid state via a transitional **liquid** state in which it intermeshes with the fibers. The resilient element is formed by **curing** **curable** elastomer in contact with the fibrous material while injecting gas formed by converting blowing agent. The gas causes the voids and cells to be formed in the intermediary layers of the resilient element. One microelectronic element is especially an electric interposer including terminals and a flexible **dielectric** film. The other includes a **semiconductor chip**.

USE - For providing a compliant interface between microelectronic elements such as a **semiconductor chip** and a substrate while making a microelectronic **package**.

ADVANTAGE - The adhesive is resistant to delamination from the resilient element under the stress of temperature, humidity, and thermal cycling.

DESCRIPTION OF DRAWING(S) - The figure shows a side view of a microelectronic **package** having the resilient element.

Resilient element 22

**dielectric** film 24

electrically conductive terminals 30

leads 32

**chip** 54

**chip** contacts 58

adhesive 60

Dwg.1/18

TECH US 6030856 A UPTX: 20000613

TECHNOLOGY FOCUS - POLYMERS - The curable adhesive is a solvent-free snap-curing adhesive such as ABLEBOND 967-3. The elastomer used to form the resilient element is a silicone elastomer such as SYLGARD 577.

FS CPI EPI

FA AB; GI

MC CPI: A06-A00E2; A08-R08A; A11-B06A; A11-B09A1; A11-C01C; A11-C02A; A11-C02D; A12-E07; A12-E07C; A12-S04A3; A12-S08D2; L04-C17D

EPI: U11-C05; U11-E02

DRN 1846-U; 1852-U; 2035-U

PLE UPA 20010116

[1.1] 018; H0124-R; P1445-R F81 Si 4A; S9999 S1309-R; L9999 L2391; L9999 L2073; M9999 M2073

[1.2] 018; B9999 B4988-R B4977 B4740; B9999 B4024 B3963 B3930 B3838 B3747; N9999 N6086

[1.3] 018; ND01; ND07; N9999 N5721-R; N9999 N7192 N7023; N9999 N6042-R; Q9999 Q7330-R; Q9999 Q7476 Q7330; Q9999 Q7818-R; K9892; K9574 K9483; K9676-R; K9698 K9676; B9999 B5301 B5298 B5276; B9999 B4682 B4568; B9999 B4717 B4706 B4568; K9701 K9676

[1.4] 018; A999 A260-R

[1.5] 018; A999 A419; S9999 S1183 S1161 S1070; S9999 S1194 S1161 S1070; S9999 S1070-R  
 [2.1] 018; R01852-R G3634 D01 D03 D11 D10 D23 D22 D31 D42 D50 D76 D86 F24 F29 F26 F34 H0293 P0599 G3623; R24078 R01852 G3634 G3623 D01 D03 D11 D10 D23 D22 D31 D42 D50 D76 D86 F24 F29 F26 F34 H0293 P0599; A999 A782; A999 A419; S9999 S1070-R; S9999 S1183 S1161 S1070; S9999 S1194 S1161 S1070  
 [2.2] 018; R00964 G0044 G0033 G0022 D01 D02 D12 D10 D51 D53 D58 D83; A999 A782; A999 A419; S9999 S1070-R; S9999 S1183 S1161 S1070; S9999 S1194 S1161 S1070; H0000; P1150; P1343  
 [2.3] 018; A999 A782; A999 A419; S9999 S1070-R; S9999 S1183 S1161 S1070; S9999 S1194 S1161 S1070; P0635-R F70 D01  
 [3.1] 018; P0000; L9999 L2391; L9999 L2073; M9999 M2073  
 [3.2] 018; Q9999 Q6644-R  
 [3.3] 018; ND01; ND07; N9999 N5721-R; N9999 N7192 N7023; N9999 N6042-R; Q9999 Q7330-R; Q9999 Q7476 Q7330; Q9999 Q7818-R; K9892; K9574 K9483; K9676-R; K9698 K9676; B9999 B5301 B5298 B5276; B9999 B4682 B4568; B9999 B4717 B4706 B4568; K9701 K9676  
 [3.4] 018; A999 A419; S9999 S1183 S1161 S1070; S9999 S1194 S1161 S1070; S9999 S1070-R

L8 ANSWER 4 OF 7 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD  
 AN 1999-492848 [41] WPIX  
 DNN N1999-367025 DNC C1999-144324  
 TI Production of **semiconductor chip assembly** with enhanced encapsulation and reduced stress.  
 DC A35 A85 L03 U11  
 IN DISTEFANO, T H  
 PA (TESS-N) TESSERA INC  
 CYC 1  
 PI US 5937276 A 19990810 (199941)\* 13p H01L021-44 <--  
 ADT US 5937276 A Provisional US 1996-33075P 19961213, US 1997-947180 19971008  
 PRAI US 1996-33075P 19961213; US 1997-947180 19971008  
 IC ICM H01L021-44  
 ICS H01L021-48; H01L021-50  
 AB US 5937276 A UPAB: 19991011  
 NOVELTY - A **semiconductor chip assembly** having enhanced encapsulation is formed by providing a support with a **dielectric** layer and an overlying bus (32) to which leads (44) are attached. A **chip** (50) is brought up, the leads detached from the bus and bonded to the contacts (54) and a **liquid** flowed between **chip** and support and **cured**.  
 DETAILED DESCRIPTION - Manufacture of a **semiconductor chip assembly** comprises providing a connection component including a support having a **dielectric** top surface and central (26) and peripheral (28) portions with a gap (20). A bus (32) overlies the periphery and gaps of the support and electrical leads (44) overlie the top surface having one end secured to the central portion and the other to the bus. A **chip** (50) is placed with its front, contact, face opposed to the bottom of the support, leads are detached and displaced from the bus and bonded to the contacts (54) and a **curable liquid** is flowed between the **chip** and support, wetting the inner edge of the bus and then **cured**.  
 USE - In producing and encapsulating **semiconductor chip assemblies** (claimed) for, e.g., TAB processes  
 ADVANTAGE - Strains and stresses on the **chip assembly** are reduced and encapsulation protects against corrosion.  
 DESCRIPTION OF DRAWING(S) - A view of the connection structure is shown.  
 Center 26  
 Periphery 28  
 Bus 32  
 Leads 44  
 Chip 50

Dwg.1/7

TECH US 5937276 A UPTX: 19991105

TECHNOLOGY FOCUS - ELECTRONICS - A protective layer is used to cover the gaps, leads have frangible sections broken during transfer and the **curable liquid** is a silicone elastomer. The bus includes a hoop-like structure of metallic bars and the support includes compliant material between the top and bottom surfaces to allow displacement of the terminals.

FS CPI EPI

FA AB; GI

MC CPI: A11-C01C; A11-C02; A12-E07C; L04-C17D; L04-C20A  
EPI: U11-E02A1

PLE UPA 19991011

[1.1] 018; S9999 S1376; M9999 M2073; L9999 L2391; L9999 L2073;  
H0124-R; P1445-R F81 Si 4A

[1.2] 018; ND07; N9999 N5721-R; B9999 B4988-R B4977 B4740; Q9999  
Q7523; Q9999 Q7476 Q7330; K9416; N9999 N7170 N7023

L8 ANSWER 5 OF 7 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD  
AN 1999-370609 [31] WPIX

CR 1996-097761 [10]; 1996-188719 [19]; 1998-007997 [01]; 1998-086369 [08];  
1998-378040 [32]; 1998-609264 [51]; 1999-384095 [30]; 1999-561109 [47];  
2000-222146 [10]; 2000-327690 [18]; 2000-338027 [25]; 2000-464036 [38];  
2000-664118 [59]; 2001-181459 [08]; 2001-624248 [49]

DNN N1999-276338

TI Method of making a compliant interface for a **semiconductor chip** and a substrate.

DC U11

IN DI STEFANO, T H; PICKETT, T; RAAB, K  
PA (TESS-N) TESSERA INC

CYC 1

PI US 5915170 A 19990622 (199931)\* 14p H01L021-44 <--

ADT US 5915170 A CIP of US 1994-309433 19940920, Div ex US 1994-365699  
19941229, Provisional US 1996-19475P 19960610, Provisional US 1997-38859P  
19970219, CIP of US 1997-842313 19970424, US 1997-931680 19970916

FDT US 5915170 A Div ex US 5659952

PRAI US 1997-931680 19970916; US 1994-309433 19940920; US 1994-365699  
19941229; US 1996-19475P 19960610; US 1997-38859P 19970219; US  
1997-842313 19970424

IC ICM H01L021-44

ICS H01L021-48; H01L021-50

AB US 5915170 A UPAB: 20011211

NOVELTY - Support pads (38) are provided by forming a mass of a **curable liquid** elastomer material using a stencil mask on the surface of a **dielectric** film (22). A **semiconductor chip** is abutted with the previously formed **dielectric** film followed by partial **curing** of elements. An encapsulant is allowed to flow between the channels of the support pads for typical **curing**.

DETAILED DESCRIPTION - The base of the support pads conforms to the shape of surface (28) of the **dielectric** film as the pads flow outward so that there are no voids between the pads and the film. Curing of the pads is carried out by using heat, UV light and another form of energy. The **dielectric** film is formed from polymeric material such as KAPTON (RTM) having a thickness of 25-75 microns. The elastomer is provided on the **dielectric** film by using a stencil mask which has several holes.

USE - For the interface between microelectronic **packaging** such as a **semiconductor chip** and a substrate.

ADVANTAGE - Prevents problems associated with thermal cycling such as voids by using support pads and adhesive pads of the same material.

DESCRIPTION OF DRAWING(S) - The figure shows a side view of a **semiconductor chip package** including the compliant interface.



dielectric film 22  
surface of dielectric film 28  
support pads 38  
Dwg.1/11

FS EPI  
FA AB; GI  
MC EPI: U11-E02A3

L8 ANSWER 6 OF 7 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD  
AN 1998-007997 [01] WPIX  
CR 1996-097761 [10]; 1996-188719 [19]; 1998-086369 [08]; 1998-378040 [32];  
1998-609264 [51]; 1999-370609 [31]; 1999-384095 [30]; 1999-561109 [47];  
2000-222146 [10]; 2000-464036 [38]; 2001-168218 [17]; 2001-624248 [49]  
DNN N1998-006352 DNC C1998-002757  
TI Manufacturing a fan-out **semiconductor chip assembly** - comprises mounting and handling **chip** using surface mounting techniques, connecting **chip** on **dielectric** element with flexible leads and injecting curable resin.  
DC A85 L03 U11  
IN DISTEFANO, T H; FARACI, T; SMITH, J W  
PA (TESS-N) TESSERA INC  
CYC 1  
PI US 5688716 A 19971118 (199801)\* 16p H01L021-44 <--  
ADT US 5688716 A Div ex US 1994-271768 19940707, CIP of US 1995-440665  
19950515, US 1996-653016 19960524  
FDT US 5688716 A Div ex US 5518964  
PRAI US 1996-653016 19960524; US 1994-271768 19940707; US 1995-440665  
19950515  
IC ICM H01L021-44  
ICS H01L021-60  
AB US 5688716 A UPAB: 20011211  
Making a **semiconductor chip assembly** comprises: (a) providing a sub-assembly including a **semiconductor chip** having a front surface and having contacts on the front surface, and a **package** element attached to the **chip** so that a peripheral region of the **package** element projects outwardly away from the **chip** in horizontal directions generally parallel to the front face of the **chip**; (b) providing a **dielectric** element having top and bottom surfaces and terminals on the top surface, and positioning the **dielectric** element to overlie the sub-assembly with the top surface and terminals facing away from the **chip** and **package** element, with a central region of the **dielectric** element disposed adjacent the **chip** and with a peripheral region of the **dielectric** element carrying at least some of the terminals overlying the peripheral region of the **package** element; (c) providing first leads attached to the **chip** at one end thereof and to the **dielectric** element at the other end thereof, the first leads being electrically connected between the contacts of the **chip** and the terminals on the **dielectric** element; (d) moving the **dielectric** element and **chip** relative to one another through a predetermined displacement so that the **dielectric** element moves with a vertical component of motion away from the **chip**, and so that the first leads are bent to a configuration in which each first lead is flexible; and (e) injecting a **curable liquid** beneath the **dielectric** element and **curing** the **liquid** to form a compliant layer supporting the **dielectric** element above the **chip** and **package** element.  
USE - Used for **packaging semiconductor chip assemblies** which incorporate the **chips** together with auxiliary elements.  
ADVANTAGE - The unitary **package** can be handled and

installed using conventional surface mounting techniques; the terminals are "fanned-out" and distributed over the peripheral region of the sheet, etc., providing widely spaced terminals for ease of mounting to the substrate. It also has good resistance to thermal stress and/or differential expansion and contraction.

Dwg.4/15

FS CPI EPI

FA AB; GI

MC CPI: A11-B05D; A11-C02C; A12-E04; A12-E07C; L04-C20D; L04-C21  
EPI: U11-D01A; U11-D02B

PLE UPA 20011211

[1.1] 018; H0328; M9999 M2073; L9999 L2391; L9999 L2073; S9999 S1434  
[1.2] 018; ND01; ND07; N9999 N5721-R; K9483-R; K9676-R; Q9999 Q7476  
Q7330; Q9999 Q7454 Q7330  
[1.3] 018; N9999 N6484-R N6440; B9999 B3838-R B3747; B9999 B4035 B3930  
B3838 B3747; B9999 B4988-R B4977 B4740  
[2.1] 018; P0464-R D01 D22 D42 F47  
[2.2] 018; ND01; ND07; N9999 N5721-R; K9483-R; K9676-R; Q9999 Q7476  
Q7330; Q9999 Q7454 Q7330  
[2.3] 018; Q9999 Q6644-R; B9999 B5527 B5505  
[3.1] 018; P0000; S9999 S1581  
[3.2] 018; ND01; ND07; N9999 N5721-R; K9483-R; K9676-R; Q9999 Q7476  
Q7330; Q9999 Q7454 Q7330  
[3.3] 018; B9999 B4035 B3930 B3838 B3747; B9999 B3203-R B3190

L8 ANSWER 7 OF 7 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD  
AN 1992-294249 [36] WPIX  
DNN N1992-225421

TI Insulated lead frame for **semiconductor packaged**  
circuits - has first and second lead fingers with power supply buses and  
insulating strip of polyimide adhesive with curing.

DC U11 U14

IN LIM, T B

PA (TEXI) TEXAS INSTR INC; (LIMT-I) LIM T B

CYC 8

PI EP 501830 A2 19920902 (199236)\* EN 14p H01L023-495 <--  
R: DE FR GB IT NL  
US 5146312 A 19920908 (199239) 12p H01L023-48 <--  
JP 06132456 A 19940513 (199424) 9p H01L023-50 <--  
EP 501830 A3 19930922 (199509) H01L023-495 <--  
EP 501830 B1 19980107 (199806) EN 17p H01L023-495 <--  
R: DE FR GB IT NL

DE 69223825 E 19980212 (199812)

SG 69957 A1 20000125 (200015)

H01L023-495 <--  
H01L023-48 <--

ADT EP 501830 A2 EP 1992-301742 19920228; US 5146312 A US 1991-662085  
19910228; JP 06132456 A JP 1992-43612 19920228; EP 501830 A3 EP  
1992-301742 19920228; EP 501830 B1 EP 1992-301742 19920228; DE 69223825 E  
DE 1992-623825 19920228, EP 1992-301742 19920228; SG 69957 A1 SG 1996-3078  
19920228

FDT DE 69223825 E Based on EP 501830

PRAI US 1991-662085 19910228

REP No-SR.Pub; 4.Jnl.Ref; EP 405871; JP 01036030; JP 02246125; JP 63244747; US  
5068712

IC ICM H01L023-48; H01L023-495; H01L023-50  
ICS H01L021-60

AB EP 501830 A UPAB: 19931006

The lead frame (25) comprises two multiple lead fingers (27) and a power  
supply bus (28a,28b) lying between the lead fingers with an insulating  
strip lying on a face of the supply bus. It is located near the edge of  
the face of the bus. The strip is an adhesive tape such as polyimide tape  
and a non conductive liquid such as liquid polyimide  
which is subsequently cured.

A second power supply bus is provided with insulating strip on the  
face between the first and second lead fingers with both edges of the

. power supply busses being stepped with multiple bonding pads.  
ADVANTAGE - Reduces possibility of wire bond shorting to power supply busses.  
3/5

ABEQ US 5146312 A UPAB: 19931006

**Semiconductor chip** comprises (a) die with bonding pads centrally along face; (b) lead frame with fingers extending over die face, with two power supply buses adjacent bonding pads; (c) series of wire bonds, some crossing over top face of power supply bus, some connecting bonding pads to top faces of supply buses; (d) encapsulating part for **semiconductor** die, wire bonds and lead frame and (e) **dielectric** strips. The **dielectric** strips are along opposite edges of top face of power supply buses, leaving part uncovered so connections from some of the wire bonds may be made, reducing chance of crossing wire band from collapsing against supply bus.

USE/ADVANTAGE - Insulated lead frame for **semiconductor** packaged devices, partic. for **IC packages**. Shorting between power supply buses is minimised. No **chip** support pad is required.  
4a/5

ABEQ EP 501830 B UPAB: 19980209

The lead frame (25) comprises two multiple lead fingers (27) and a power supply bus (28a,28b) lying between the lead fingers with an insulating strip lying on a face of the supply bus. It is located near the edge of the face of the bus. The strip is an adhesive tape such as polyimide tape and a non conductive **liquid** such as **liquid** polyimide which is subsequently **cured**.

A second power supply bus is provided with insulating strip on the face between the first and second lead fingers with both edges of the power supply busses being stepped with multiple bonding pads.

ADVANTAGE - Reduces possibility of wire bond shorting to power supply busses.  
fr

Dwg.1/4a

FS EPI

FA AB; GI

MC EPI: U11-D03A1A; U14-A10

=>

2 ANSWER 1 OF 1 HCAPLUS COPYRIGHT 2002 ACS  
 AN 2001:279602 HCAPLUS  
 TI Enhancements in framed sheet processing  
 IN Beroz, Masud; Distefano, Thomas H.; Hendrickson, Matthew T.; Light,  
 David; Smith, John W.  
 PA Tessera, Inc., USA  
 SO U.S., 27 pp.  
 CODEN: USXXAM  
 DT Patent  
 LA English  
 IC ICM B32B001-04  
 ICS H01L021-02  
 NCL 428068000  
 FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6217972	B1	20010417	US 1998-173797	19981016
	US 5518964	A	19960521	US 1997-61932 P	19971017
	US 5798286	A	19980825	US 1994-271768	19940707
	US 5688716	A	19971118	US 1995-532528	19950922
				US 1996-653016	19960524 <--
	US 5913109	A	19990615	US 1994-271768 A3	19940707
				US 1995-440665 A2	19950515
				US 1996-690532	19960731
				US 1994-271768 A3	19940707
				US 1995-440665 A1	19950515
WO 9711486	A1	19970327	WO 1996-US15170	19960923	
W:	AL, AM, AT, AU, AZ, BB, BG, BR, BY, CA, CH, CN, CZ, DE, DK, EE, ES, FI, GB, GE, HU, IL, IS, JP, KE, KG, KP, KR, KZ, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, TJ, TM, TR, TT, UA, UG, UZ, VN, AM, AZ, BY, KG, KZ, MD, RU, TJ, TM				
RW:	KE, LS, MW, SD, SZ, UG, AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, BF, BJ, CF, CG, CI, CM, GA, GN				
AU 9672425	A1	19970409	US 1995-532528 A	19950922	
			AU 1996-72425	19960923	
			US 1995-532528 A	19950922	
EP 853816	A1	19980722	WO 1996-US15170W	19960923	
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W:	AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, DE, DK, EE, ES, FI, GB, GE, GH, GM, GW, HU, ID, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, UA, UG, UZ, VN, YU, ZW, AM, AZ, BY, KG, KZ, MD, RU, TJ, TM				
RW:	GH, GM, KE, LS, MW, SD, SZ, UG, ZW, AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG				
AU 9862374	A1	19980717	US 1996-32828 P	19961213	
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			US 1994-271768 A3	19940707	
			US 1994-366236 B2	19941229	
			US 1995-440665 A2	19950515	
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US 1997-61932 P 19971017  
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AB A flexible sheet used in manufacture of microelectronic components is held on a frame formed from a rigid material so that the frame maintains the sheet under tension during processing and thereby stabilizes the dimensions of the sheet. The frame may be formed from a rigid, light-transmissive material such as a glass, and the bond between the frame and sheet may be made or released by light transmitted through the frame. Preferred features of the framed sheet minimize entrapment of processing liquids such as etch solutions, thereby minimizing carryover of processing solutions between steps. The frame may have contact openings which permit engagement of a metallic layer on the sheet by an electrode carrying electroplating or etching current without disturbing the main portion of the sheet where features are to be formed or treated.

RE.CNT 34

RE

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- (2) Anon; DE 3919564 A1 1991
- (3) Anon; WO 9403036 1994
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- (6) Bowling; US 3762032 1973
- (7) Boyd; US 3562058 1971
- (8) Coquin; US 4037111 1977
- (9) Destefano; US 5776796 1998
- (10) Distefano; US 5282312 1994
- (11) Distefano; US 5518964 1996

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- (17) Faraci; US 5798286 1998
- (18) Jacobs; US 5055907 1991
- (19) Johnson; US 3657805 1972
- (20) Khandros; US 5148266 1992
- (21) Kinsman; US 5336649 1994
- (22) Moden; US 6064221 2000
- (23) Moore; US 3766638 1973
- (24) Oki; US 5605844 1997
- (25) Roberts; US 5362681 1994
- (26) Schubert; US 3755048 1973
- (27) Schwartzbauer; US 5169804 1992
- (28) Smith; US 5622900 1997
- (29) Smith; US 5830782 1998
- (30) Sooriakumar; US 5578167 1996
- (31) Takeuchi; US 5238876 1993
- (32) Ueki; US 5288663 1994
- (33) Witcraft; US 5280894 1994
- (34) Wojnarowski; US 5866952 1999

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L5 2 L4 AND SEMICONDUCTOR

=> d sca ti

L5 2 ANSWERS HCAPLUS COPYRIGHT 2002 ACS  
TI Bondable compliant pads for packaging of a semiconductor chip and method therefor

HOW MANY MORE ANSWERS DO YOU WISH TO SCAN? (1):1

L5 2 ANSWERS HCAPLUS COPYRIGHT 2002 ACS  
TI Method of making chip mountings and assemblies

ALL ANSWERS HAVE BEEN SCANNED

=> d max 1-

YOU HAVE REQUESTED DATA FROM 2 ANSWERS - CONTINUE? Y/(N):y

L5 ANSWER 1 OF 2 HCAPLUS COPYRIGHT 2002 ACS  
AN 2000:142541 HCAPLUS  
TI Bondable compliant pads for packaging of a semiconductor chip and method therefor

IN Distefano, Thomas H.; Kovac, Zlata; Smith, John W.  
PA Tessaera, Inc., USA

SO U.S., 18 pp., which  
CODEN: USXXAM

DT Patent

LA English

IC ICM H01L021-44

ICS H01L021-48; H01L021-50

NCL 438117000

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6030856	A	20000229	US 1997-872379	19970610
				US 1996-19475 P	19960610
				US 1996-32722 P	19961213
				US 1996-32960 P	19961213
	US 6294040	B1	20010925	US 1997-879922	19970620
				US 1996-32722 P	19961213
				US 1996-32960 P	19961213

AB A method of making a microelectronic package includes providing first and second microelectronic elements having electrically conductive parts and disposing a resilient element having one or more intermediary layers capable of being wetted by an adhesive between the microelectronic elements. The resilient element includes fibrous material, a fibrous matrix and/or voids formed at the intermediary layers thereof. An adhesive is provided between the intermediary layers and the microelectronic elements. The adhesive is then cured while it remains in contact with the intermediary layers for bonding the resilient element and the microelectronic elements. The electrically conductive parts are then bonded together to form electrical interconnections. A microelectronic package comprising a resilient element including one or more intermediary layers capable of being wetted by an adhesive is also provided.

RE.CNT 19

RE

- (1) Anon; RU 1003396 1980
- (2) Baker; US 5405807 1995
- (3) Beckham; US 4604644 1986
- (4) Chance; US 3614832 1971
- (5) Dibble; US 5316788 1994
- (6) Distefano; US 5548091 1996
- (7) Grabbe; US 4642889 1987

- (8) Grube; US 5414298 1995
- (9) Kandros; US 5148266 1992
- (10) Kovacs; US 5659952 1997
- (11) Lakritz; US 4545610 1985
- (12) Luttmer; US 3795037 1974
- (13) Marcantonio; US 4710798 1987
- (14) Nellis; US 3680037 1972
- (15) Ohao; US 4237607 1980
- (16) Schueller; US 5663530 1997
- (17) Sweis; US 5477611 1995
- (18) Tessier; US 5661088 1997
- (19) Zifcak; US 4793814 1988

L5 ANSWER 2 OF 2 HCAPLUS COPYRIGHT 2002 ACS  
 AN 1999:761597 HCAPLUS  
 TI Method of making chip mountings and assemblies  
 IN Smith, John W.; Distefano, Thomas H.  
 PA Tessera, Inc, USA  
 SO U.S., 15 pp., Cont.-in-part of Ser. No. US 1996-695875, filed on 13 Aug  
 1996 which  
 CODEN: USXXAM  
 DT Patent  
 LA English  
 IC ICM H01L021-00  
 NCL 438689000  
 FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
US 5994222	A	19991130	US 1997-845786	19970425
			US 1996-14718	19960624
			US 1996-21479	19960703
			US 1996-695875	19960813

AB A bonding component for electrically connecting a **semiconductor chip** or wafer to a support substrate includes a dielectric layer having a central region, elongated slots defining the central region, and a peripheral region surrounding the slots. Metallic bonding pads are arranged on the central region, and leads extend from the bonding pads to the edge of the central region and extending partially across the elongated slots. The leads are detached from the peripheral region of the dielectric layer on the side of the slots opposite the central region. The leads are adapted to be deformed during bonding to a **semiconductor chip** or wafer. To form the bonding component, a dielectric layer is first provided having a central region, slots and a peripheral region. A metallic structure is also provided having bonding pads on the central region, and leads electrically connected to the bonding pads and to a plating bus disposed in the peripheral region. A resist is applied to the metallic structure in zones separating the leads, the metallic structure is plated in regions outside the zones with an etch resistant metal, the resist is removed and the leads are etched so as to form gaps in the metallic structure over the elongated slots.

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L1 ANSWER 2 OF 3 WPIX COPYRIGHT 2002 DERWENT INFORMATION LTD  
 AN 1998-007997 [01] WPIX  
 CR 1996-097761 [10]; 1996-188719 [19]; 1998-086369 [08]; 1998-378040 [32];  
 1998-609264 [51]; 1999-370609 [31]; 1999-384095 [30]; 1999-561109 [47];  
 2000-222146 [10]; 2000-464036 [38]; 2001-168218 [17]; 2001-624248 [49]  
 DNN N1998-006352 DNC C1998-002757  
 TI Manufacturing a fan-out semiconductor chip assembly - comprises mounting  
 and handling chip using surface mounting techniques, connecting chip on  
 dielectric element with flexible leads and injecting curable resin.  
 DC A85 L03 U11  
 IN DISTEFANO, T H; FARACI, T; SMITH, J W  
 PA (TESS-N) TESSERA INC  
 CYC 1  
 PI US 5688716 A 19971118 (199801)\* 16p H01L021-44  
 ADT US 5688716 A Div ex US 1994-271768 19940707, CIP of US 1995-440665  
 19950515, US 1996-653016 19960524  
 FDT US 5688716 A Div ex US 5518964  
 PRAI US 1996-653016 19960524; US 1994-271768 19940707; US 1995-440665  
 19950515  
 IC ICM H01L021-44  
 ICS H01L021-60  
 AB US 5688716 A UPAB: 20011211

Making a semiconductor chip assembly comprises: (a) providing a  
 sub-assembly including a semiconductor chip having a front surface and  
 having contacts on the front surface, and a package element attached to  
 the chip so that a peripheral region of the package element projects  
 outwardly away from the chip in horizontal directions generally parallel  
 to the front face of the chip; (b) providing a dielectric element having  
 top and bottom surfaces and terminals on the top surface, and positioning  
 the dielectric element to overlie the sub-assembly with the top surface  
 and terminals facing away from the chip and package element, with a  
 central region of the dielectric element disposed adjacent the chip and  
 with a peripheral region of the dielectric element carrying at least some  
 of the terminals overlying the peripheral region of the package element;  
 (c) providing first leads attached to the chip at one end thereof and to  
 the dielectric element at the other end thereof, the first leads being  
 electrically connected between the contacts of the chip and the terminals  
 on the dielectric element; (d) moving the dielectric element and chip  
 relative to one another through a predetermined displacement so that the  
 dielectric element moves with a vertical component of motion away from the  
 chip, and so that the first leads are bent to a configuration in which  
 each first lead is flexible; and (e) injecting a curable liquid beneath  
 the dielectric element and curing the liquid to form a compliant layer  
 supporting the dielectric element above the chip and package element.  
 USE - Used for packaging semiconductor chip assemblies which  
 incorporate the chips together with auxiliary elements.

ADVANTAGE - The unitary package can be handled and installed using  
 conventional surface mounting techniques; the terminals are "fanned-out"  
 and distributed over the peripheral region of the sheet, etc., providing  
 widely spaced terminals for ease of mounting to the substrate. It also has  
 good resistance to thermal stress and/or differential expansion and  
 contraction.

Dwg.4/15

FS CPI EPI  
 FA AB; GI

MC CPI: A11-B05D; A11-C02C; A12-E04; A12-E07C; L04-C20D; L04-C21  
 EPI: U11-D01A; U11-D02B  
 PLE UPA 20011211

[1.1] 018; H0328; M9999 M2073; L9999 L2391; L9999 L2073; S9999 S1434  
 [1.2] 018; ND01; N9999 N5721-R; K9483-R; K9676-R; Q9999 Q7476  
 Q7330; Q9999 Q7454 Q7330  
 [1.3] 018; N9999 N6484-R N6440; B9999 B3838-R B3747; B9999 B4035 B3930  
 B3838 B3747; B9999 B4988-R B4977 B4740

[2.1] 018; P0464-R D01 D22 D42 F47  
[2.2] 018; ND01; ND07; N9999 N5721-R; K9483-R; K9676-R; Q9999 Q7476  
Q7330; Q9999 Q7454 Q7330  
[2.3] 018; Q9999 Q6644-R; B9999 B5527 B5505  
[3.1] 018; P0000; S9999 S1581  
[3.2] 018; ND01; ND07; N9999 N5721-R; K9483-R; K9676-R; Q9999 Q7476  
Q7330; Q9999 Q7454 Q7330  
[3.3] 018; B9999 B4035 B3930 B3838 B3747; B9999 B3203-R B3190